

FIG. 1a

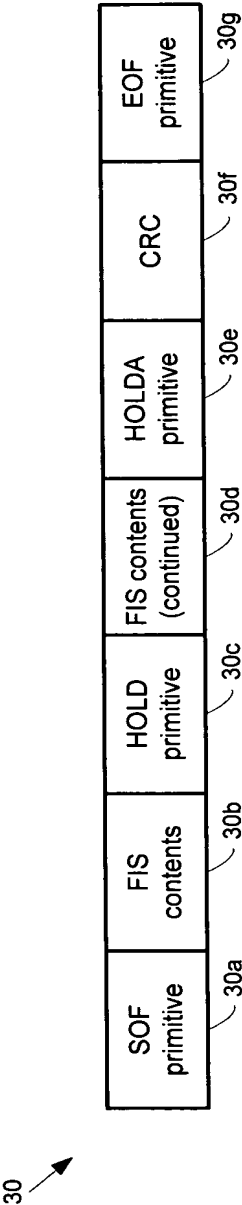


FIG. 1b

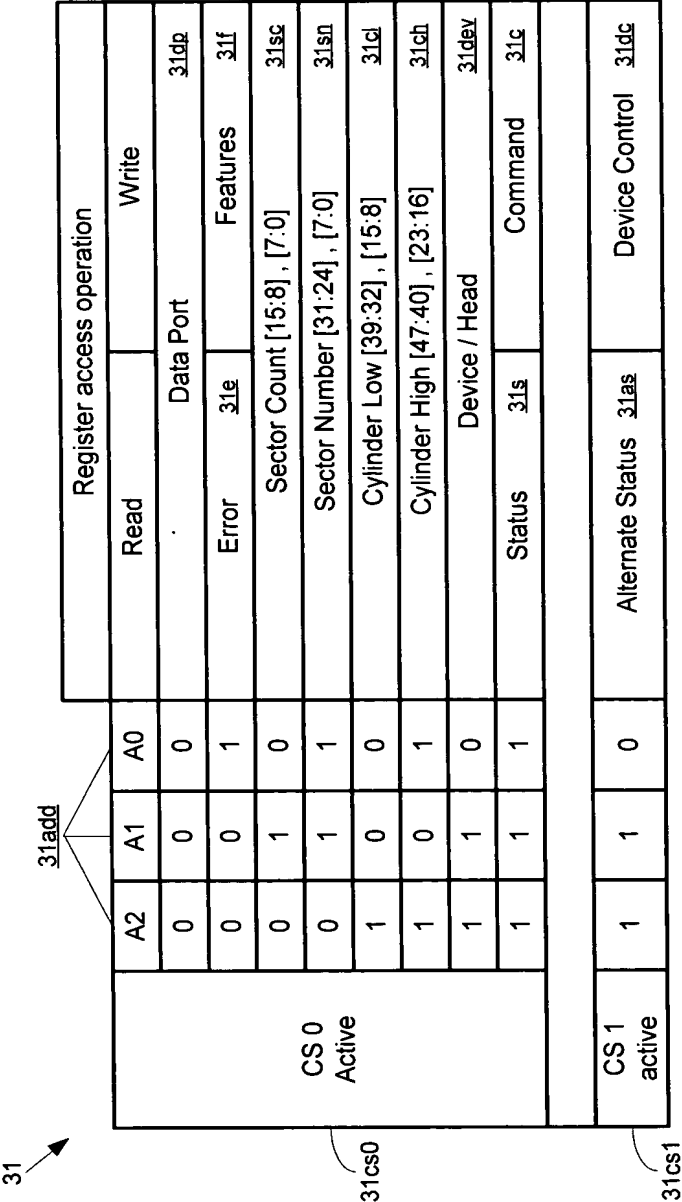


FIG. 1c

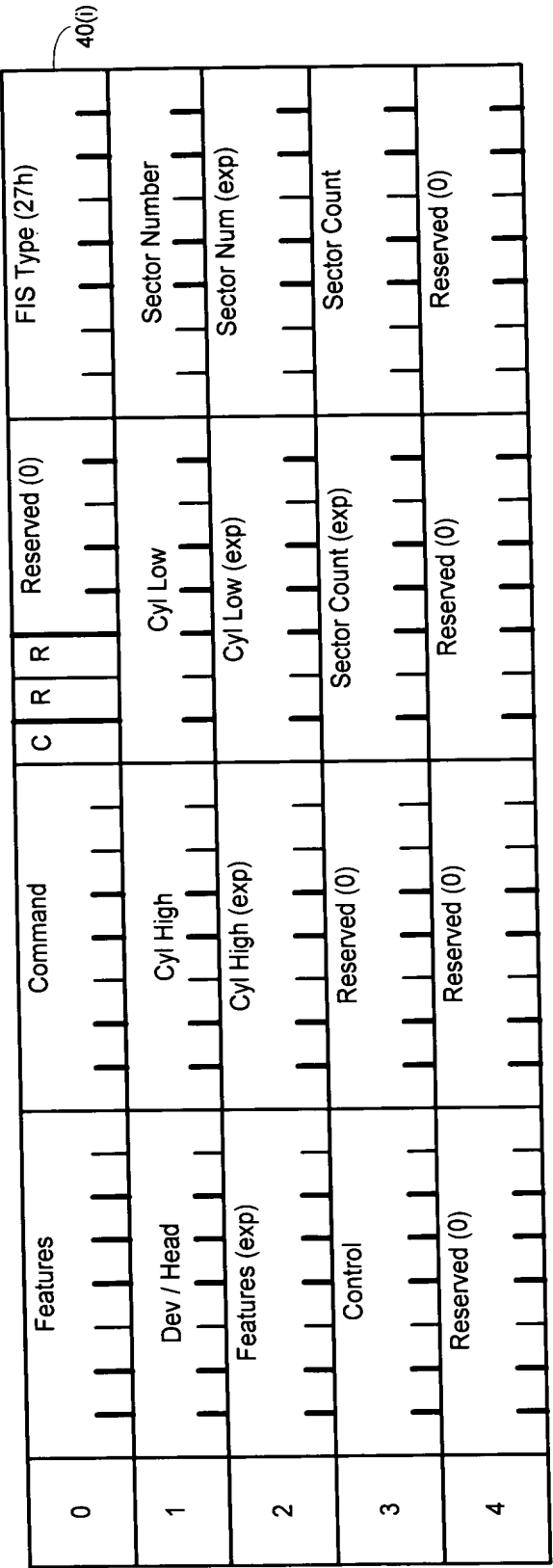


FIG. 1d(i) Register FIS Host to Device

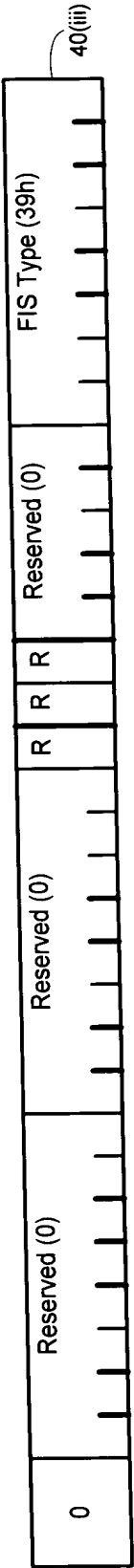


FIG. 1d(iii) DMA Activate FIS, Device to Host

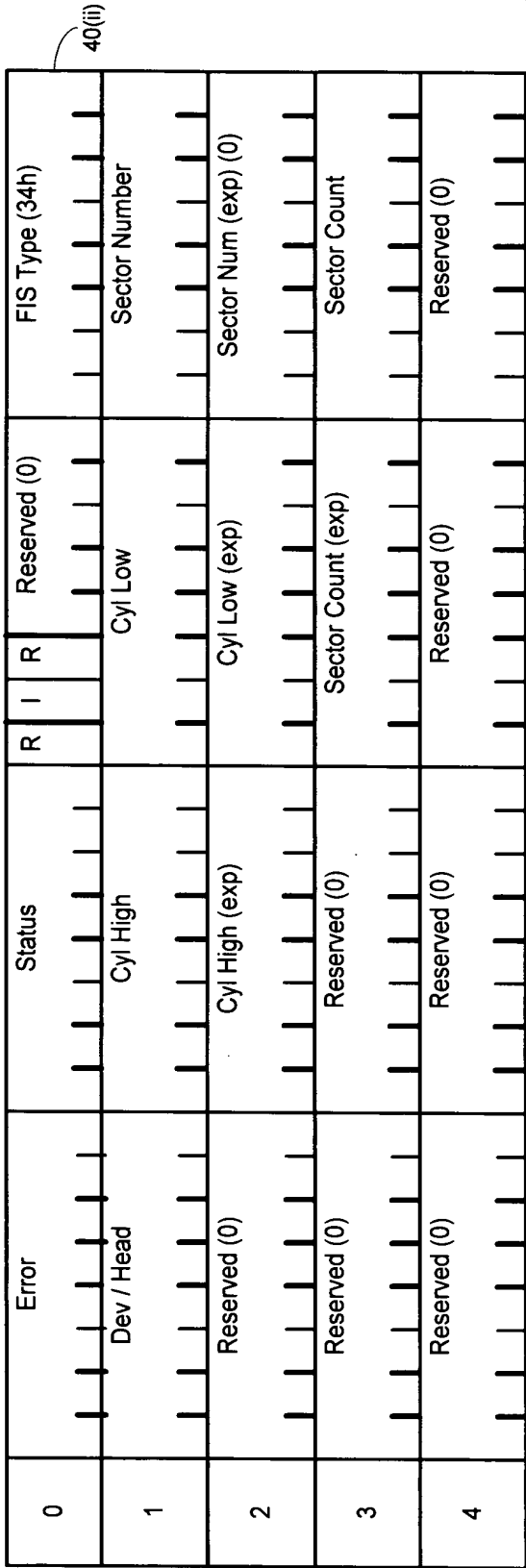


FIG. 1d(ii) Register FIS Device to Host

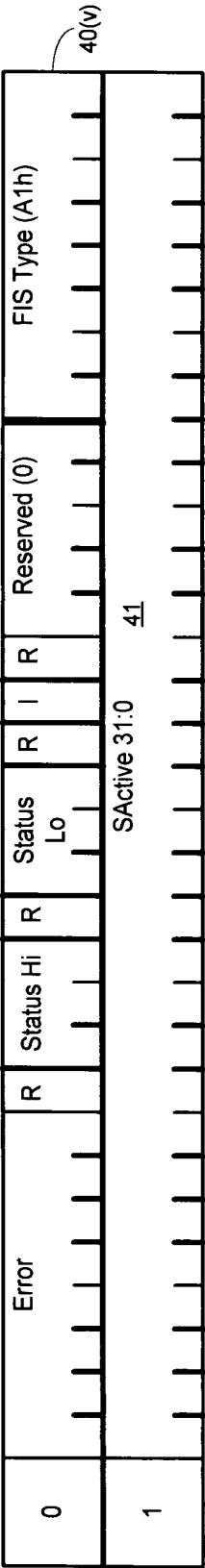


FIG. 1d(v) Set Device Bits FIS

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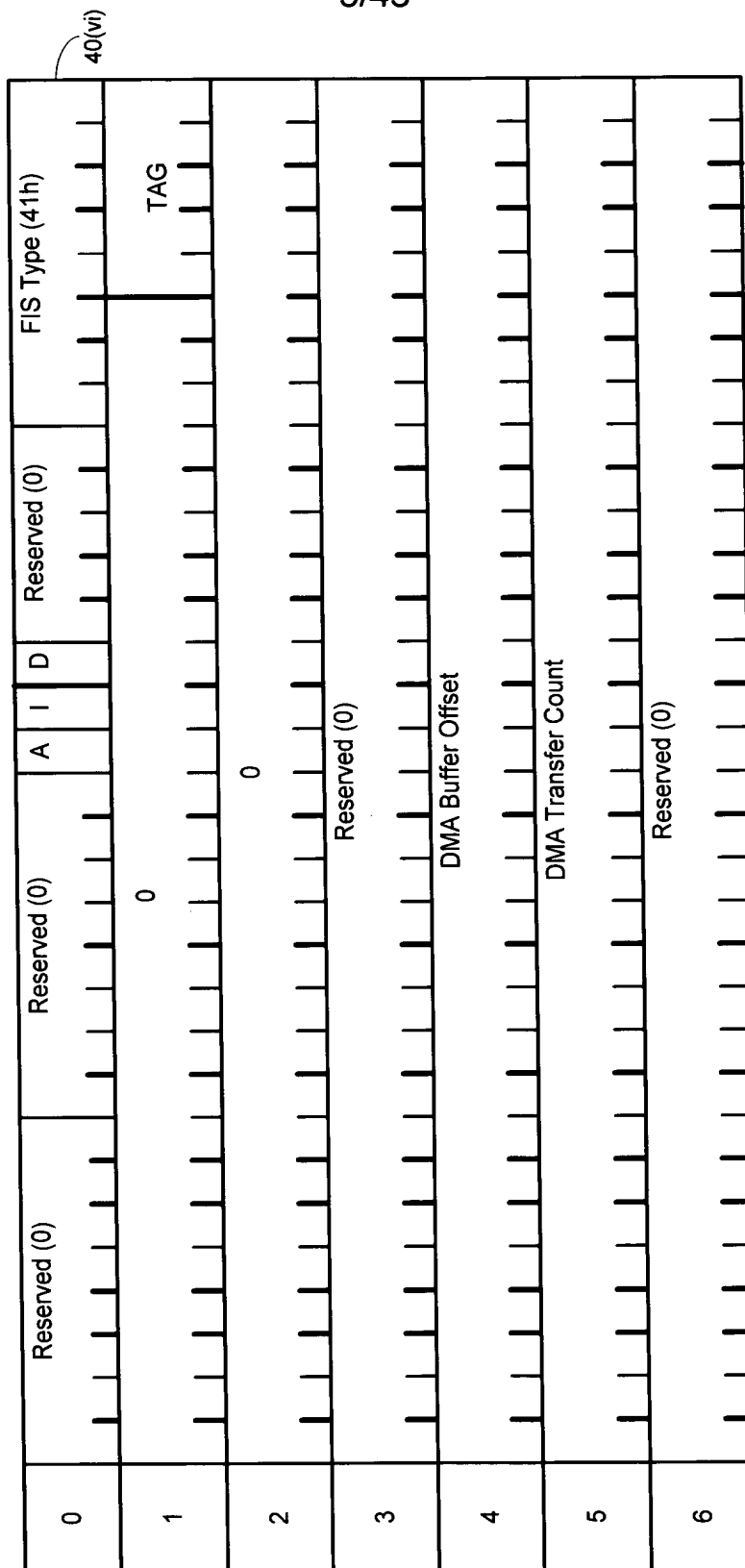


FIG. 1d(iv) DMA Setup FIS

0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Reserved (0)	Cyl High (exp)	Cyl Low (exp)				Sector Number (exp) (0)
3	E_Status	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)		Transfer Count				

FIG. 1d (vi) PIO Setup FIS

0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)						
...							
n							

FIG. 1d(vii) Data FIS

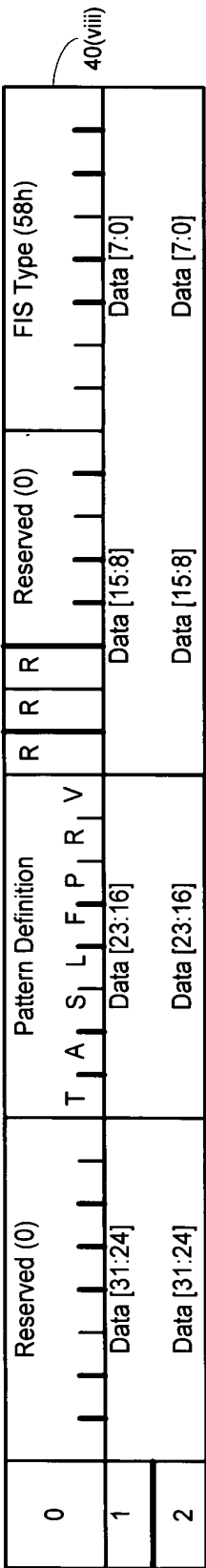


FIG. 1d (viii) BIST Activate FIS

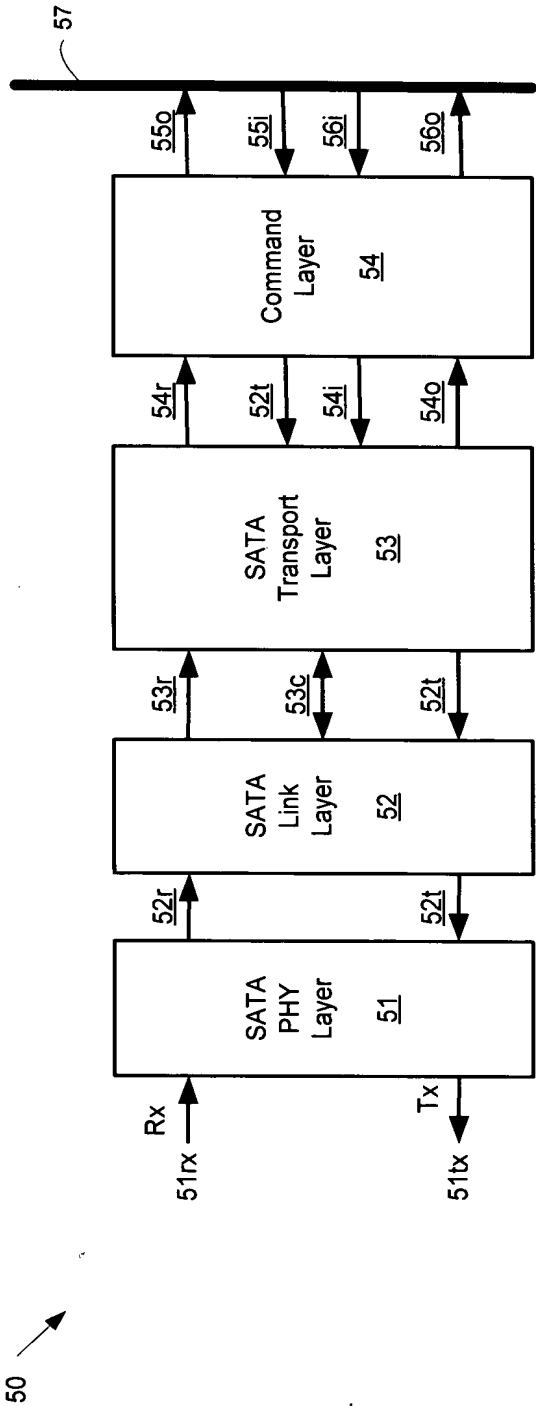


FIG. 2a

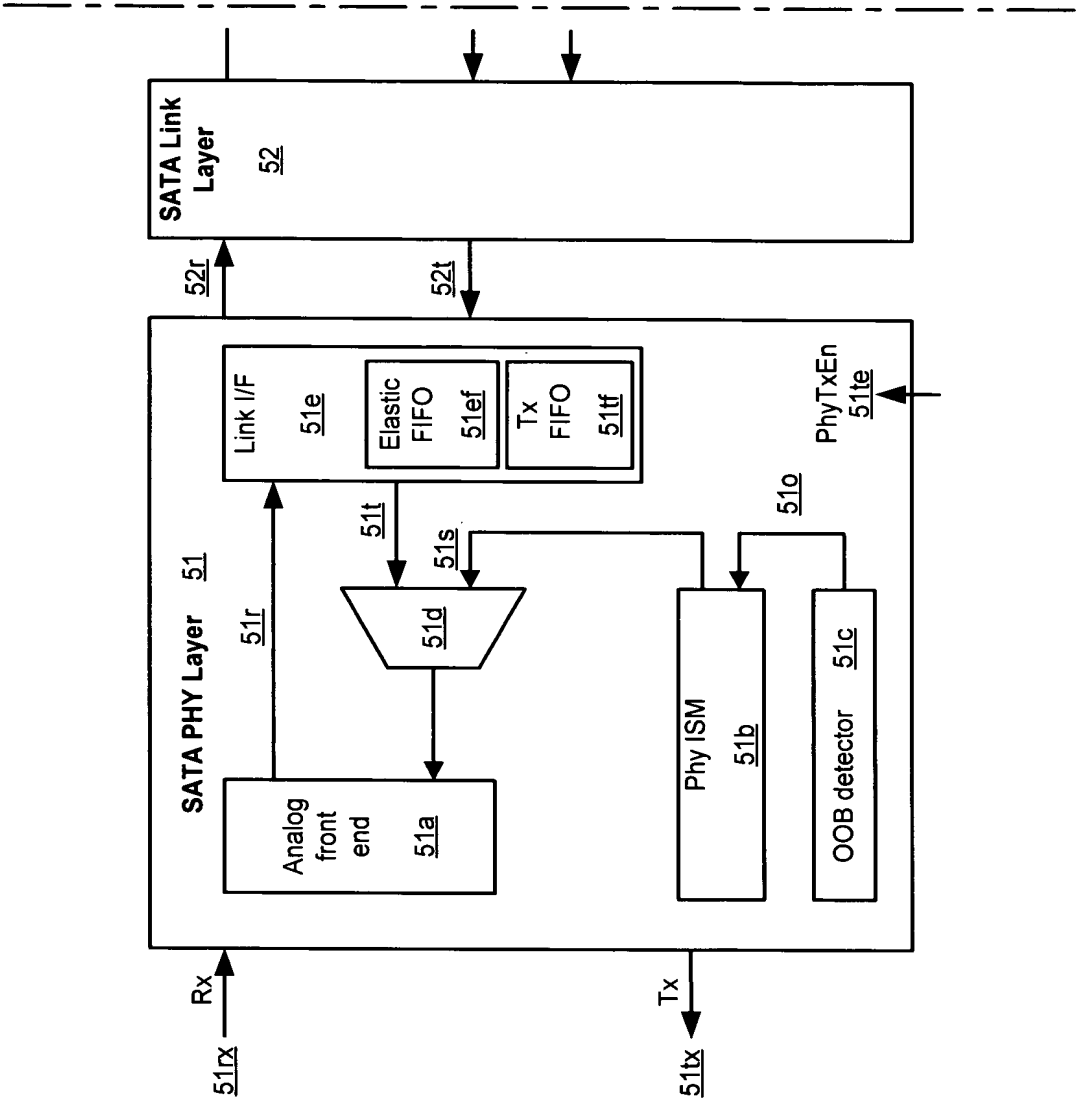


FIG. 2b(i)

Fig. 2b(i)	Fig. 2b(ii)
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Key To  
FIG. 2b



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↙

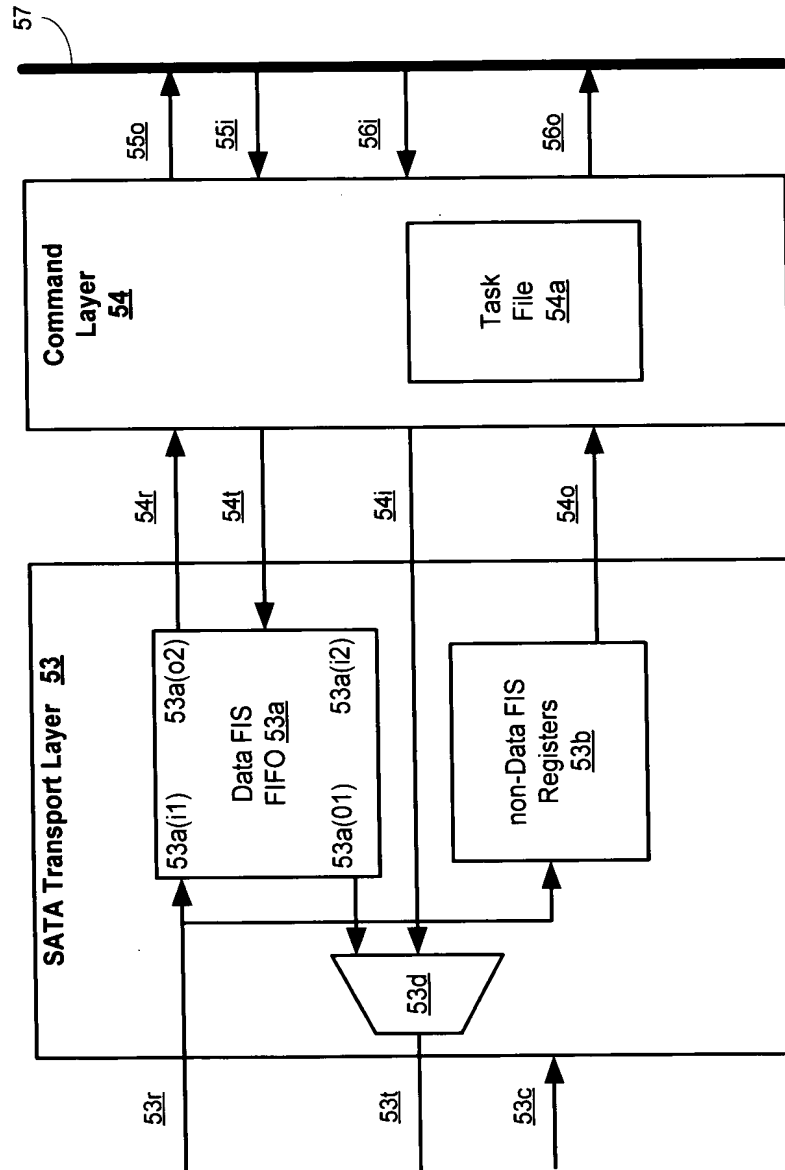


FIG. 2b(ii)

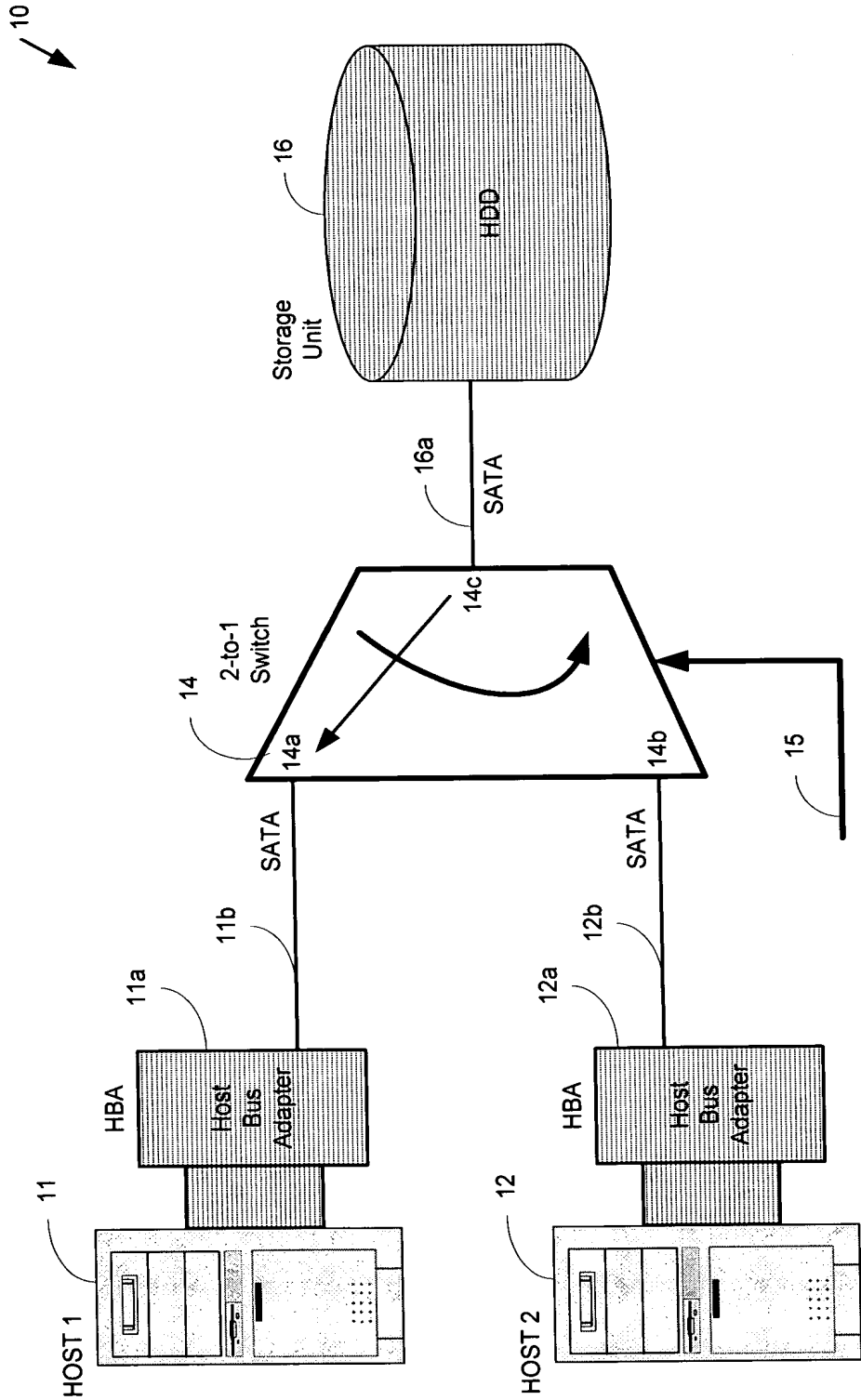


FIG. 3a

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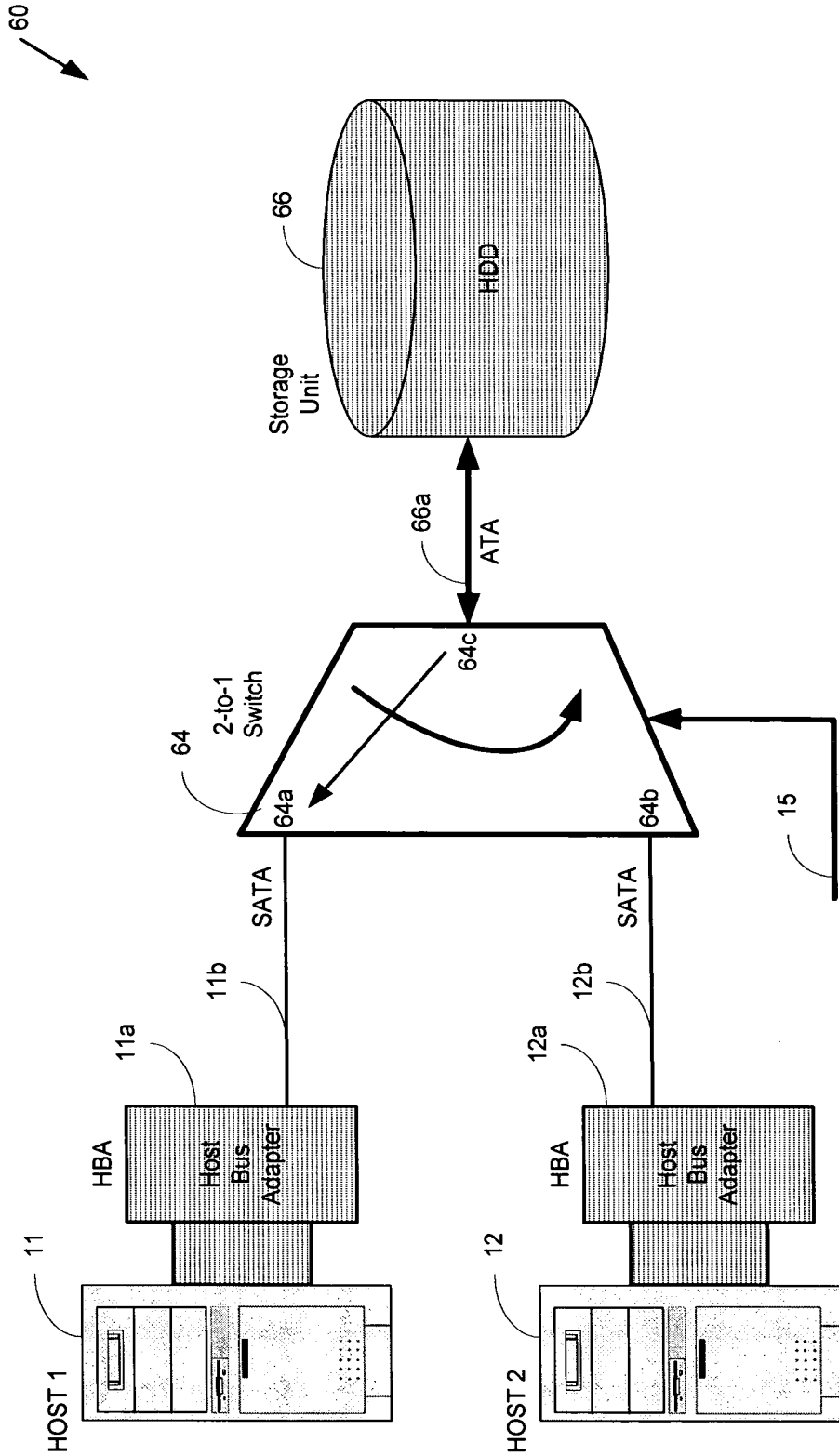


FIG. 3b

FIG. 4a      FIG. 4b

Key To

FIG. 4

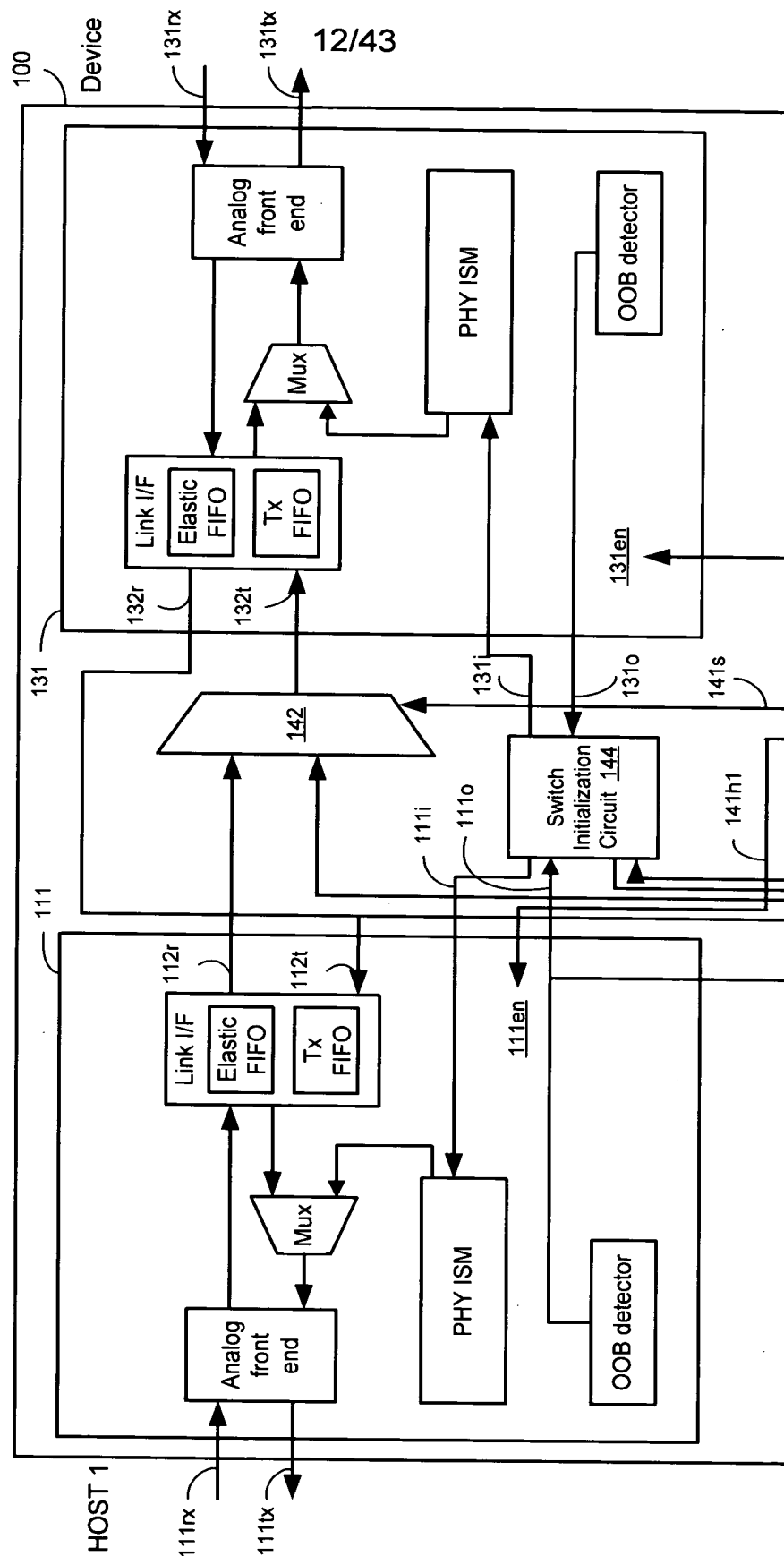


FIG. 4a

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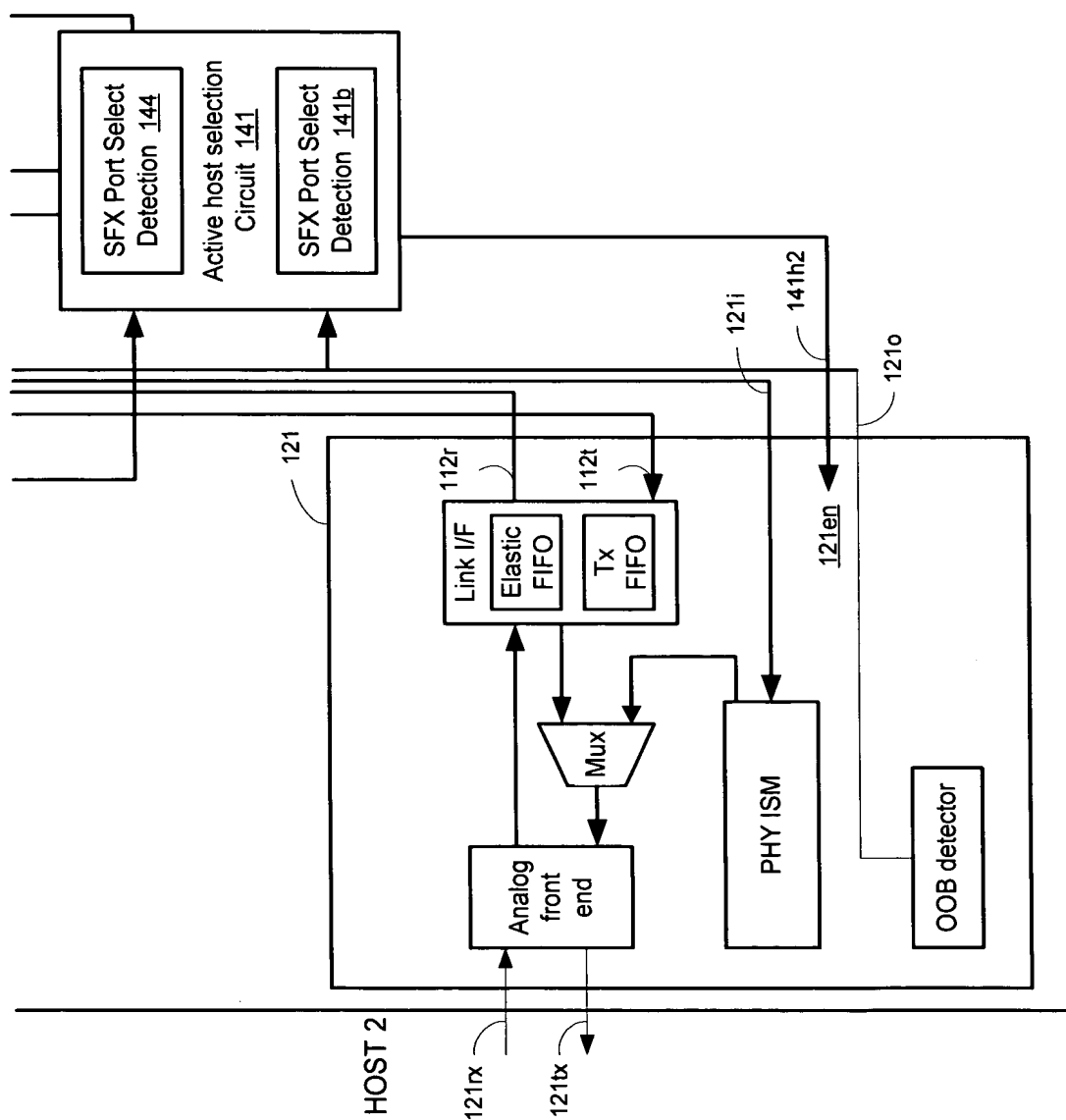


FIG. 4b

FIG. 5a	FIG. 5b
FIG. 5c	Key To FIG. 5

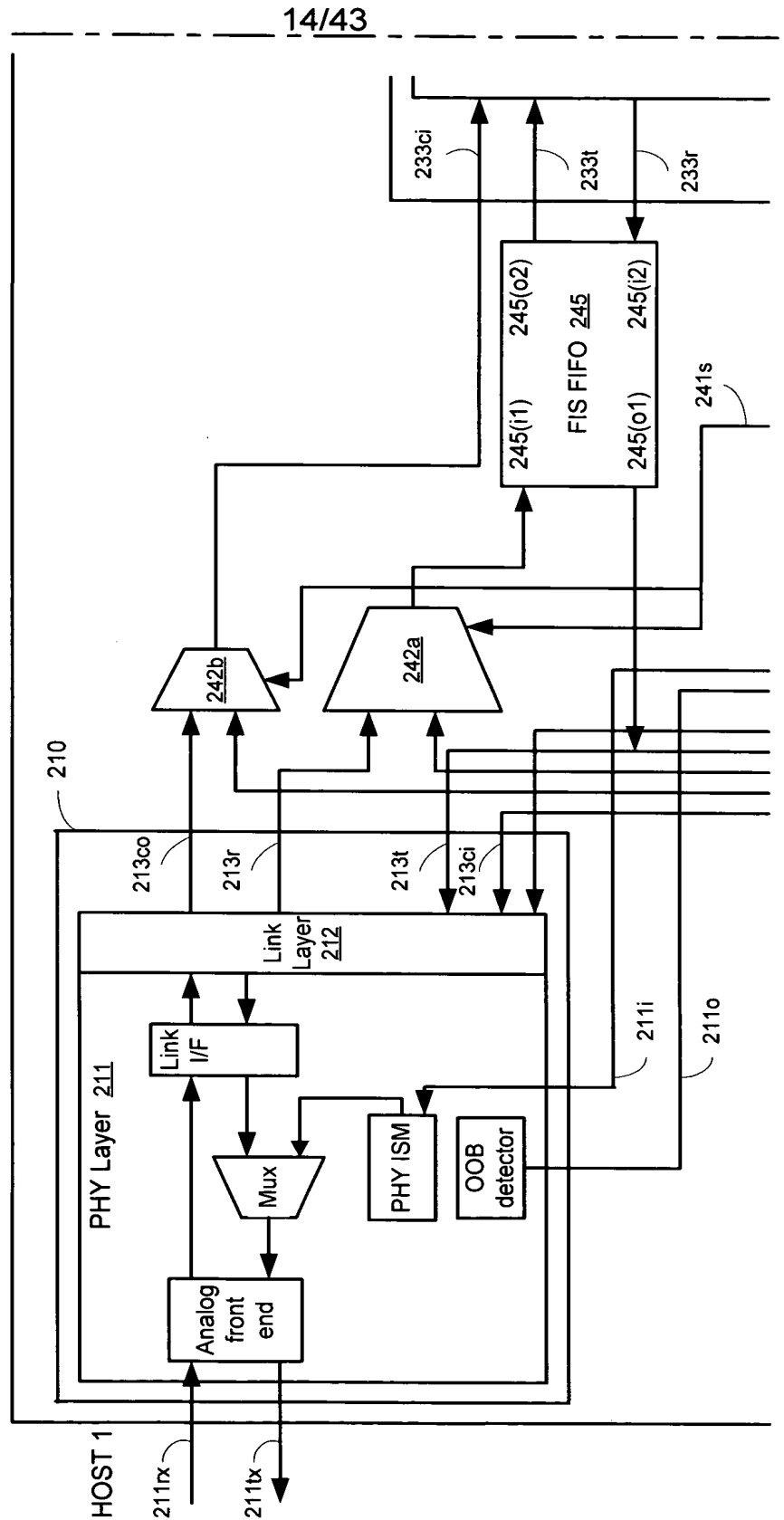


FIG. 5a

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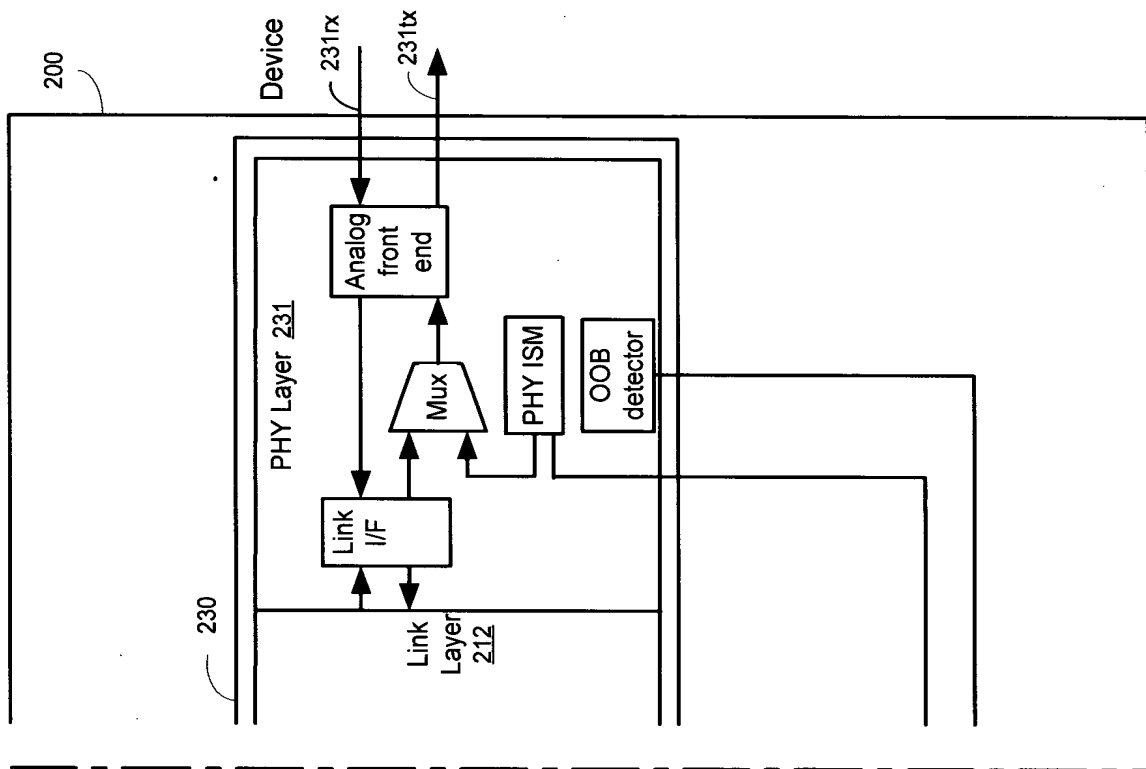


FIG. 5b

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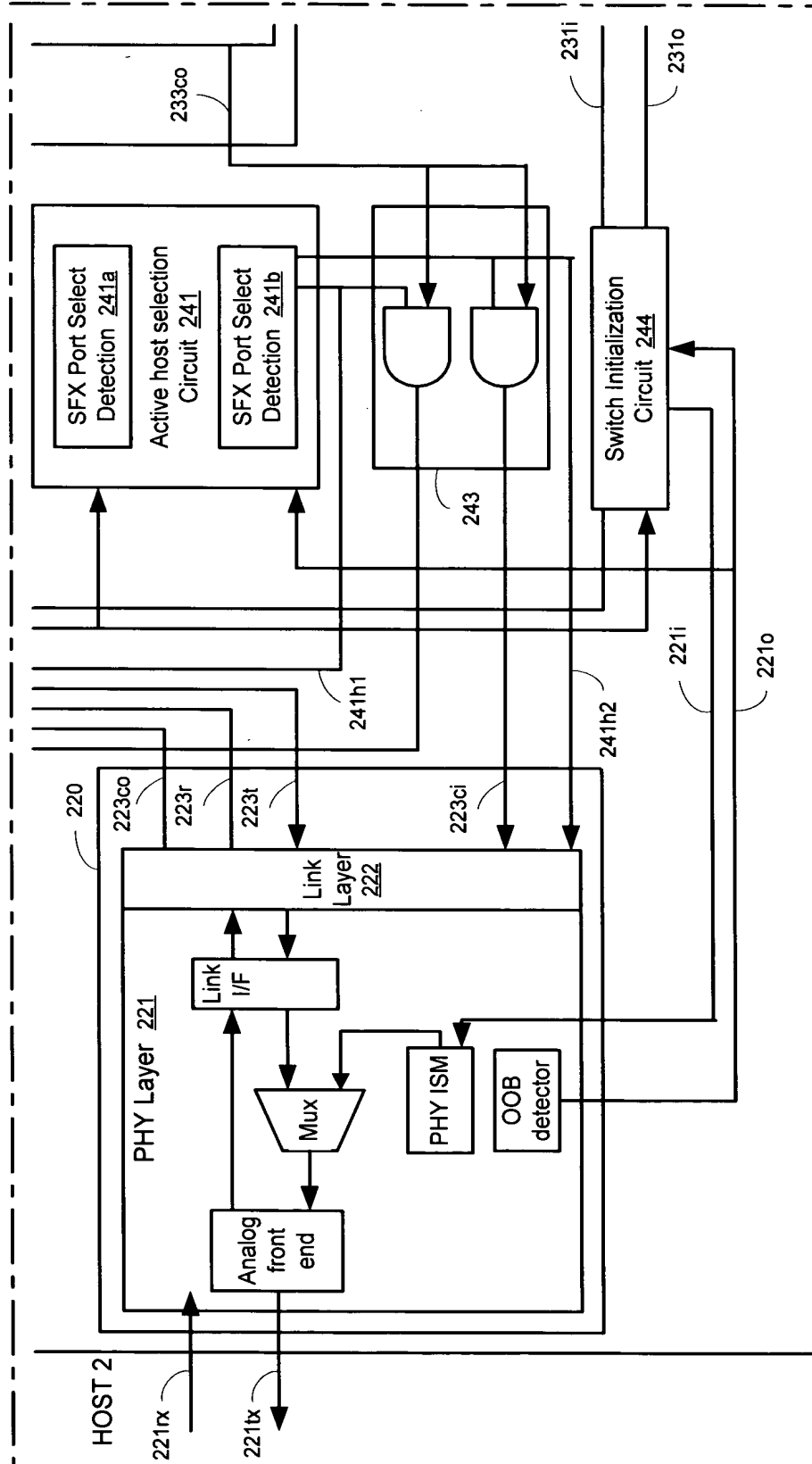


FIG. 5c



FIG. 6a      FIG. 6b

Key To  
FIG. 6

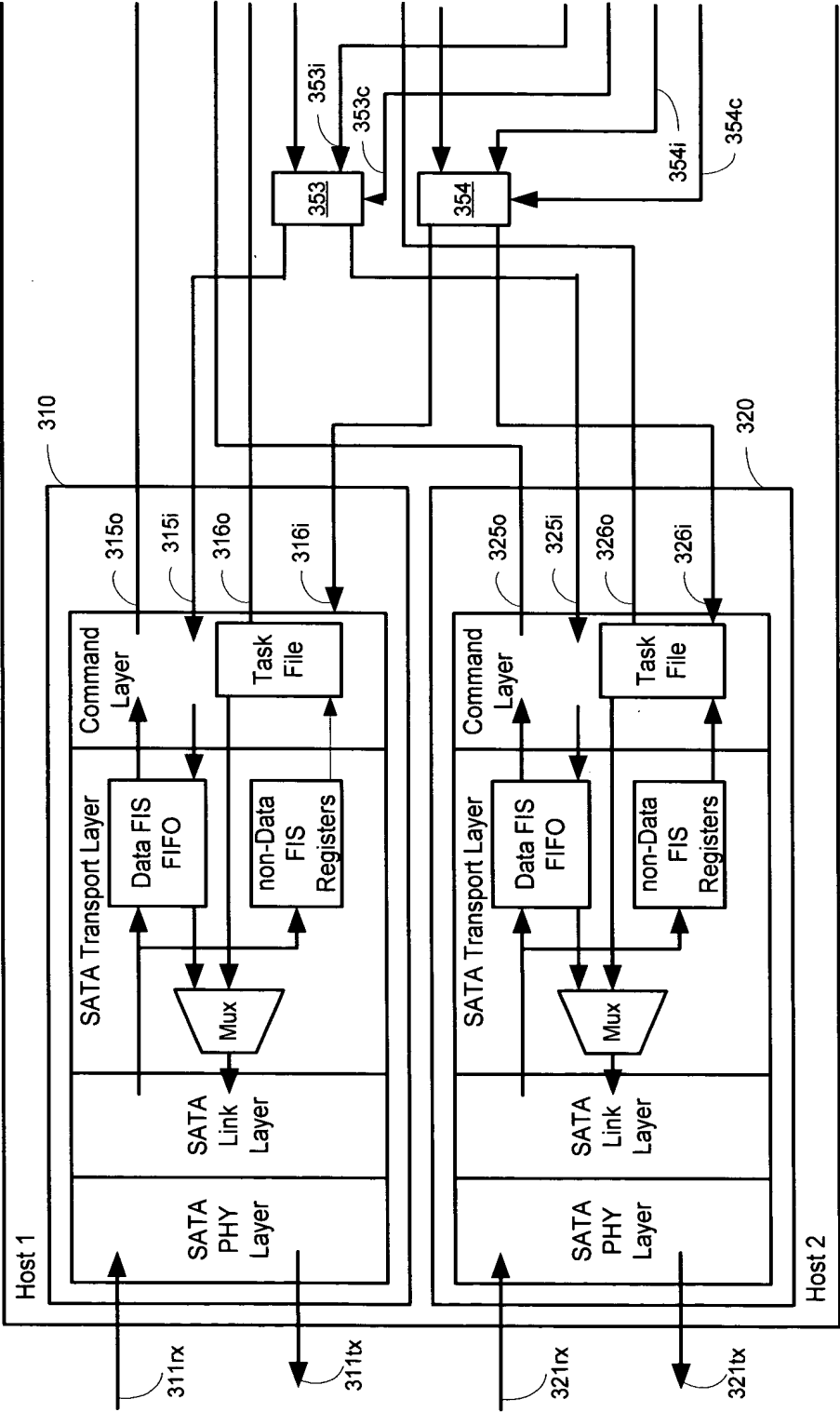


FIG. 6a

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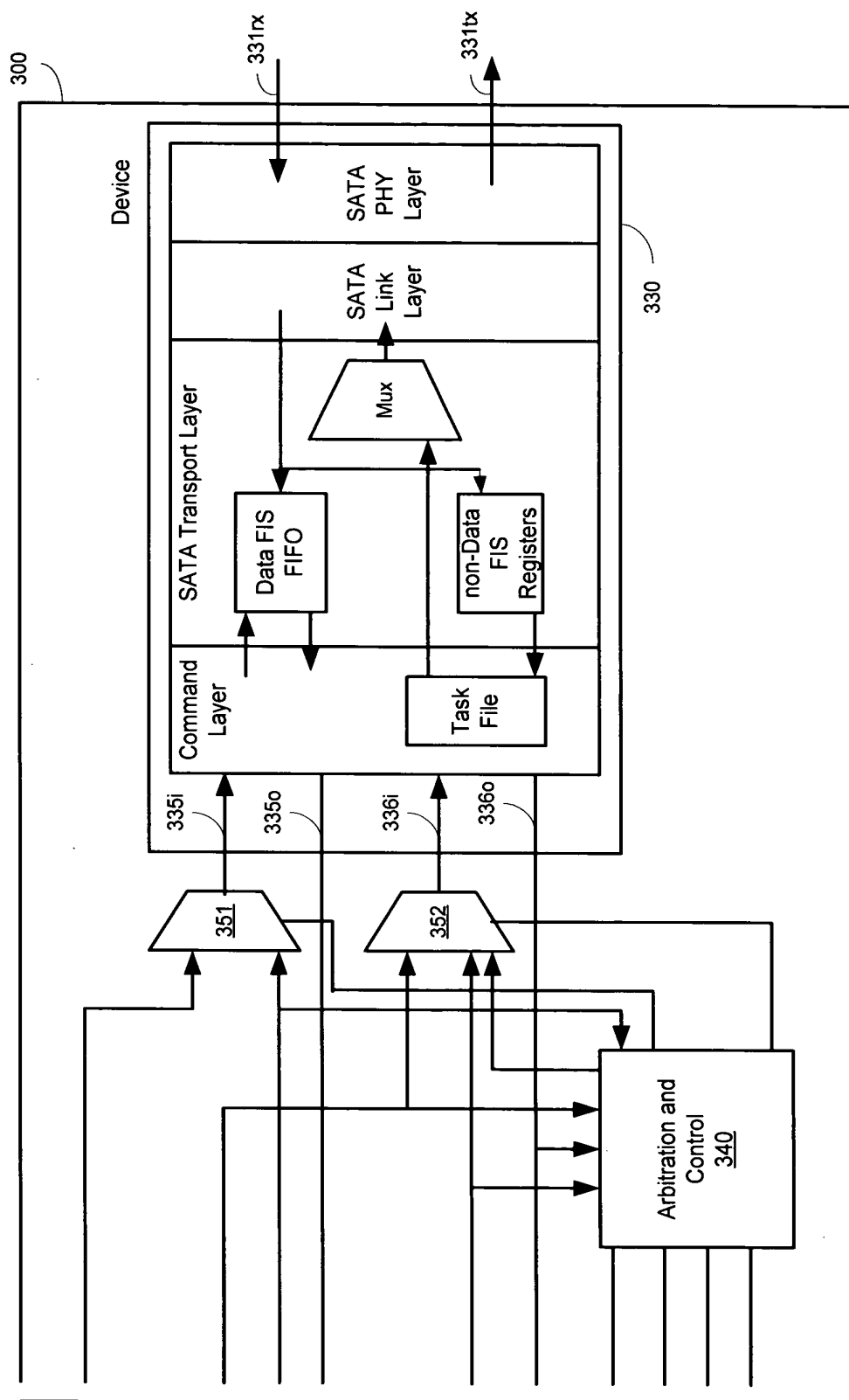


FIG. 6b

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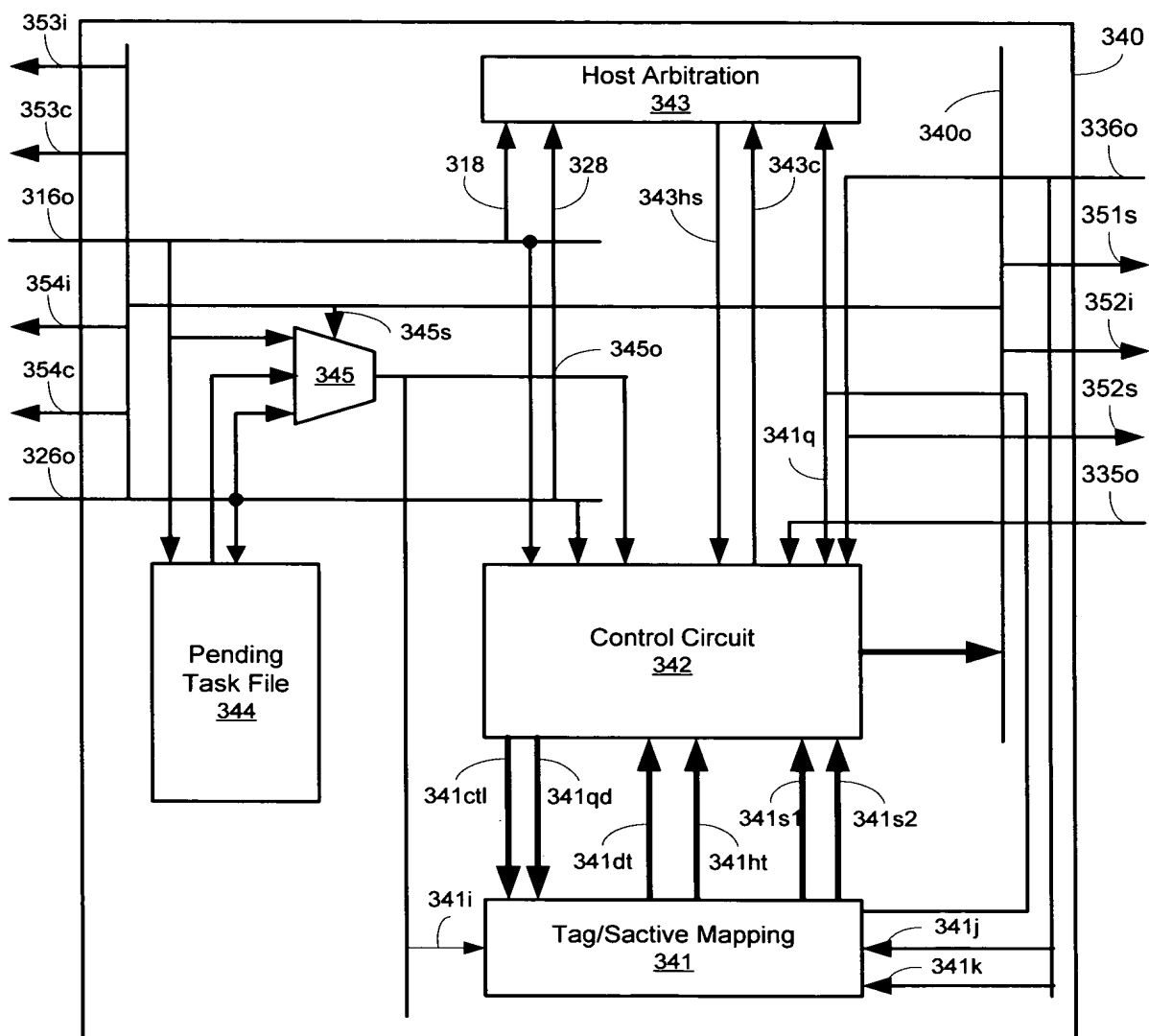


FIG. 7a

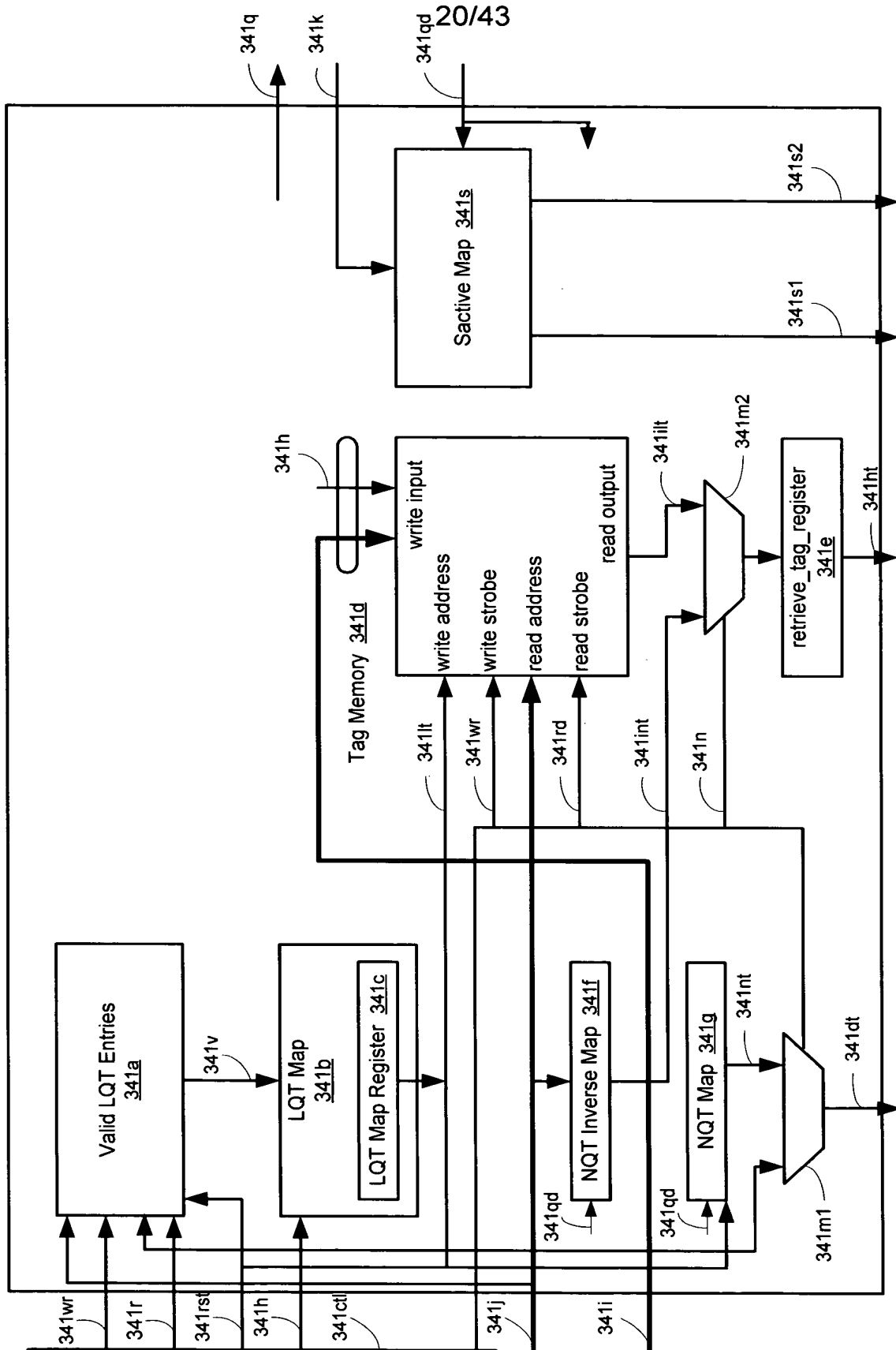


FIG. 7b

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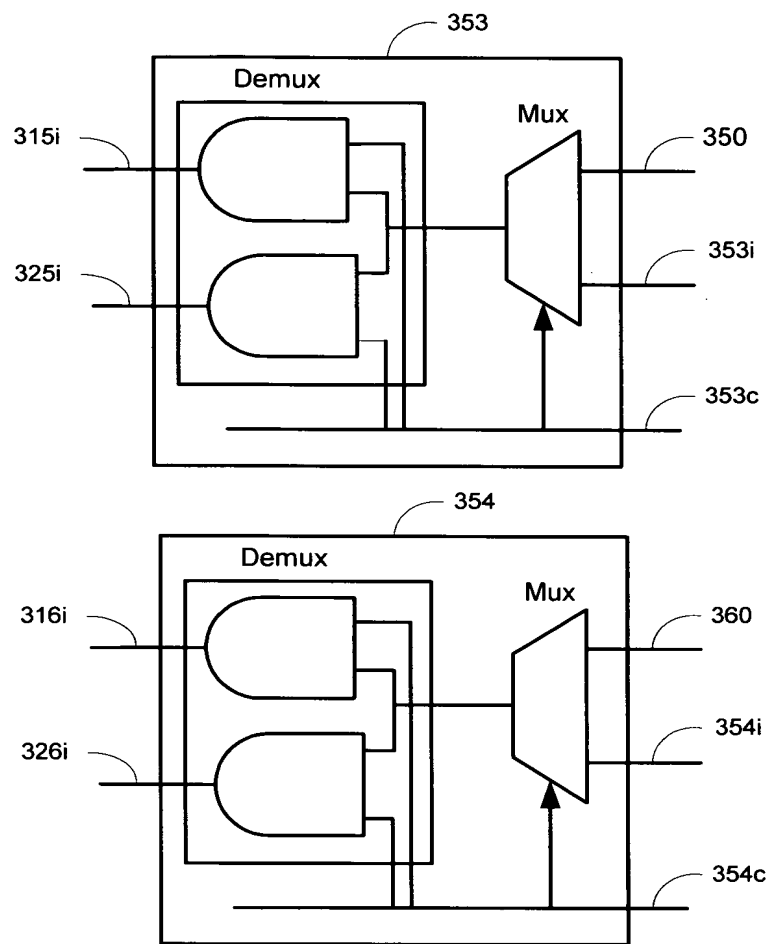


FIG. 7c

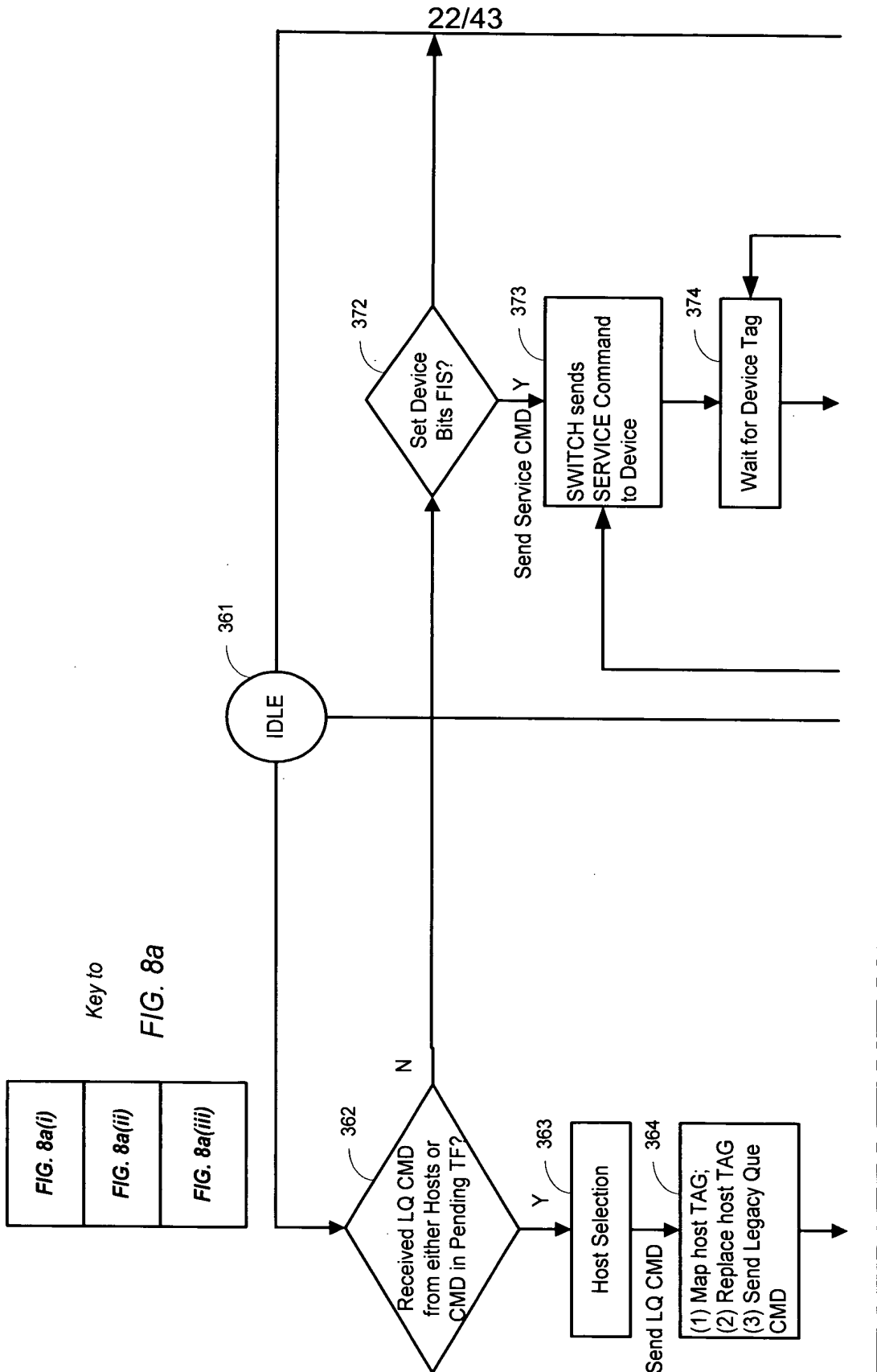


FIG. 8a(i)

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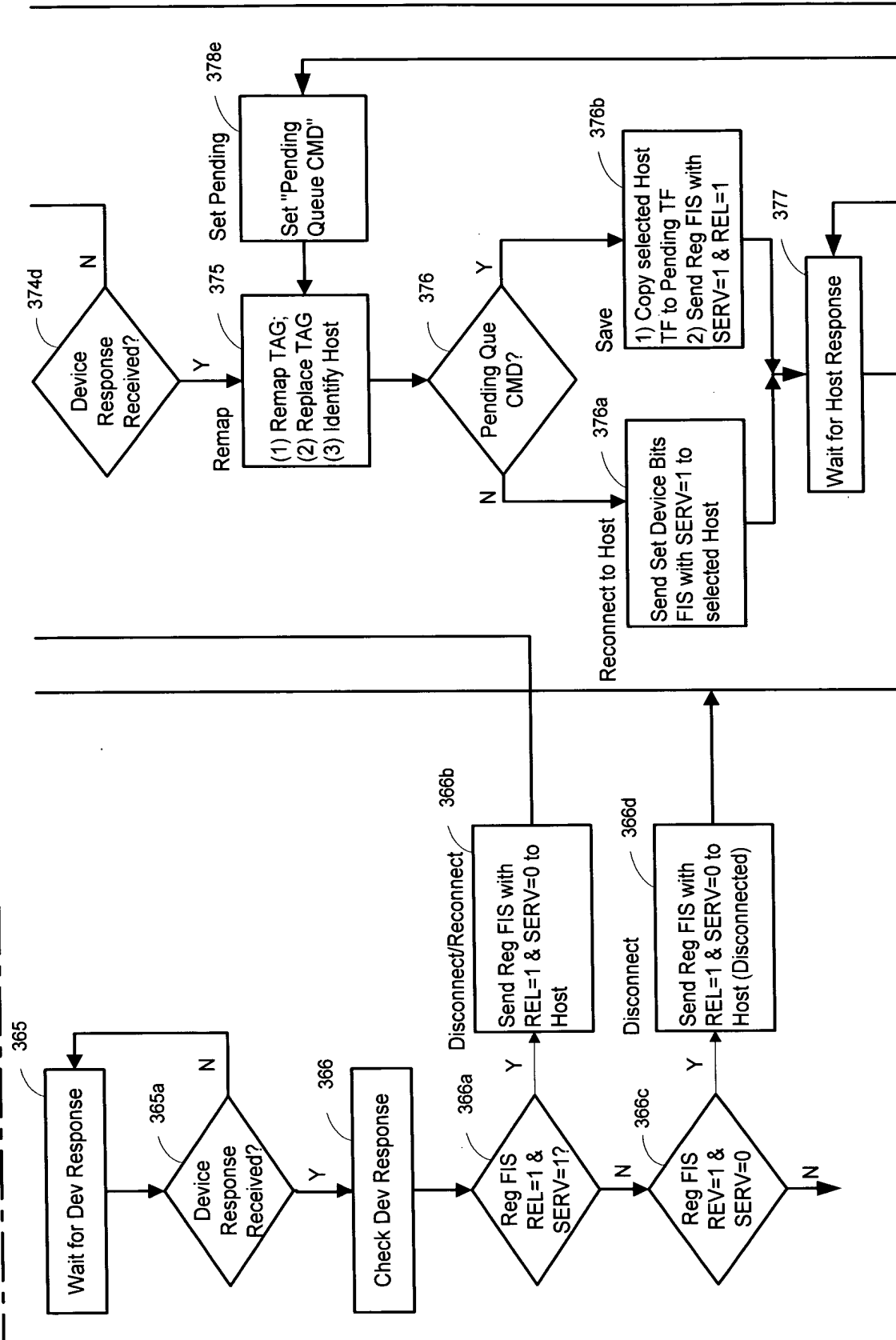


FIG. 8a(ii)

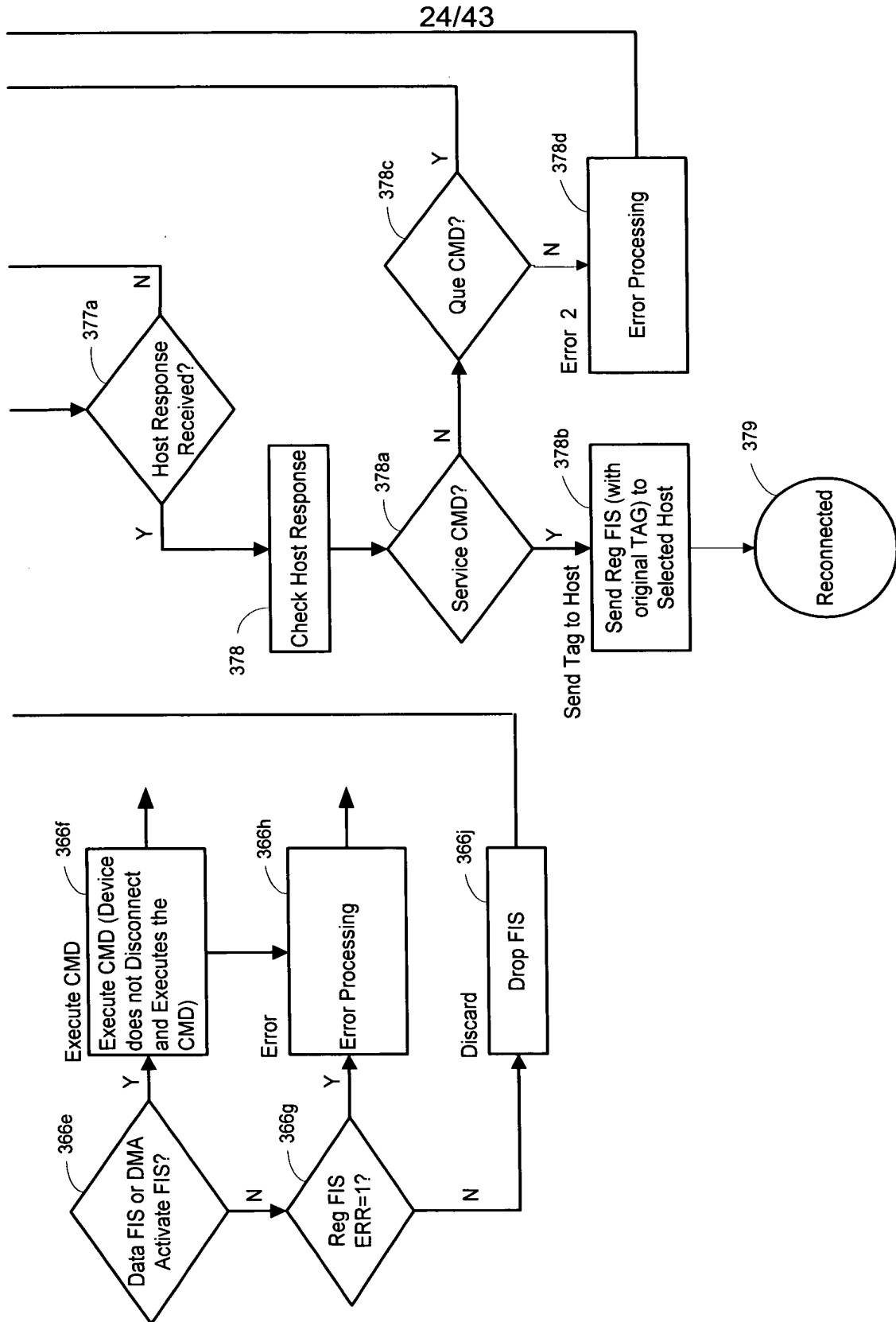


FIG. 8a(iii)



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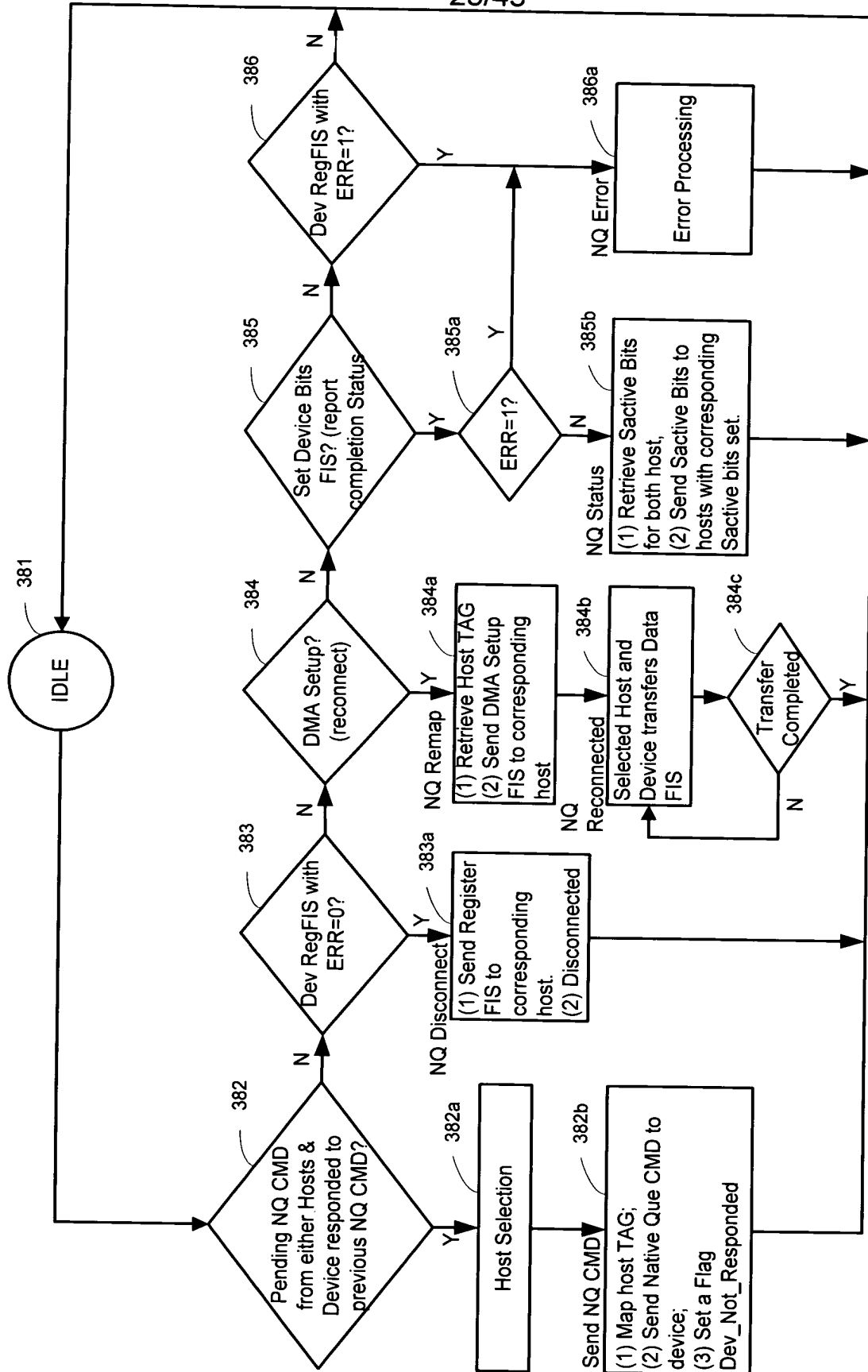


FIG. 8b

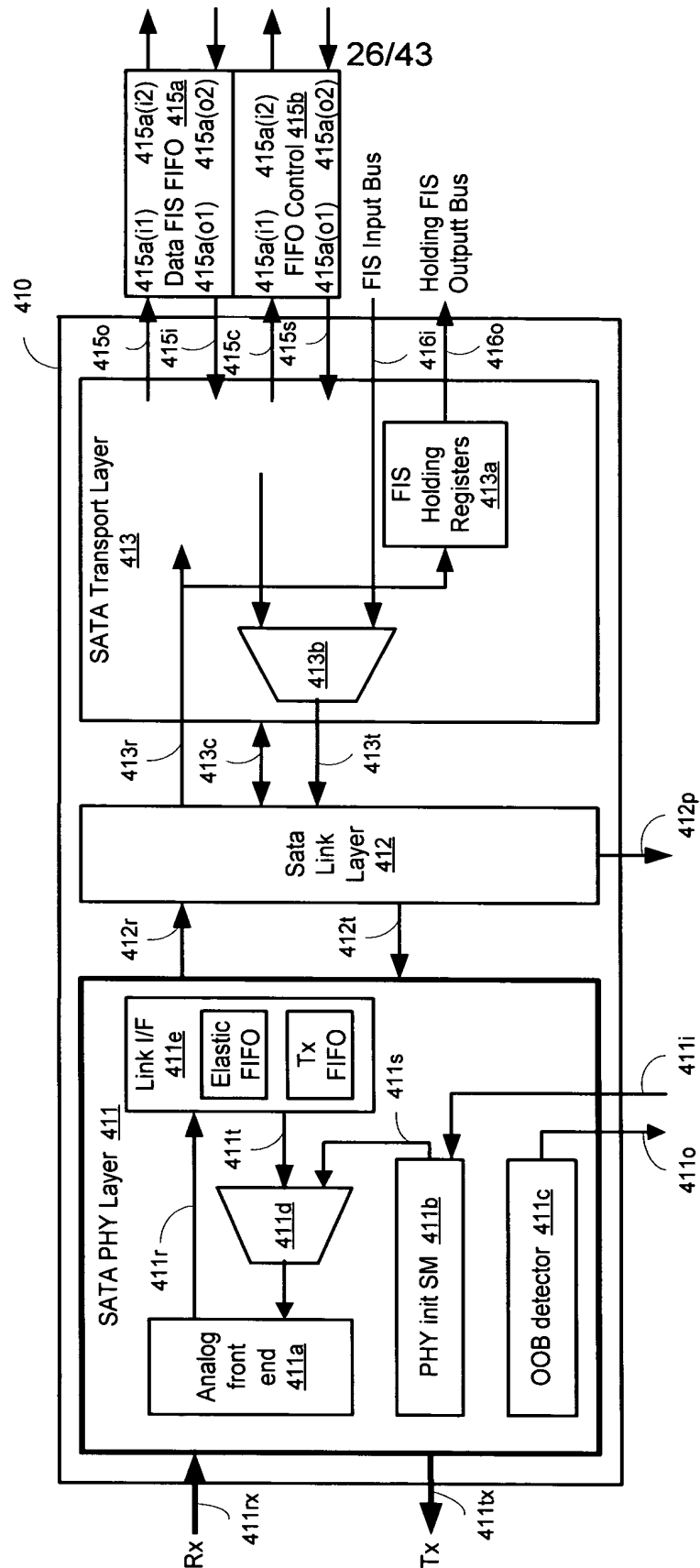


FIG. 9

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FIG. 10a(i)	FIG. 10a(ii)	FIG. 10a(iii)
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Key to

FIG. 10a

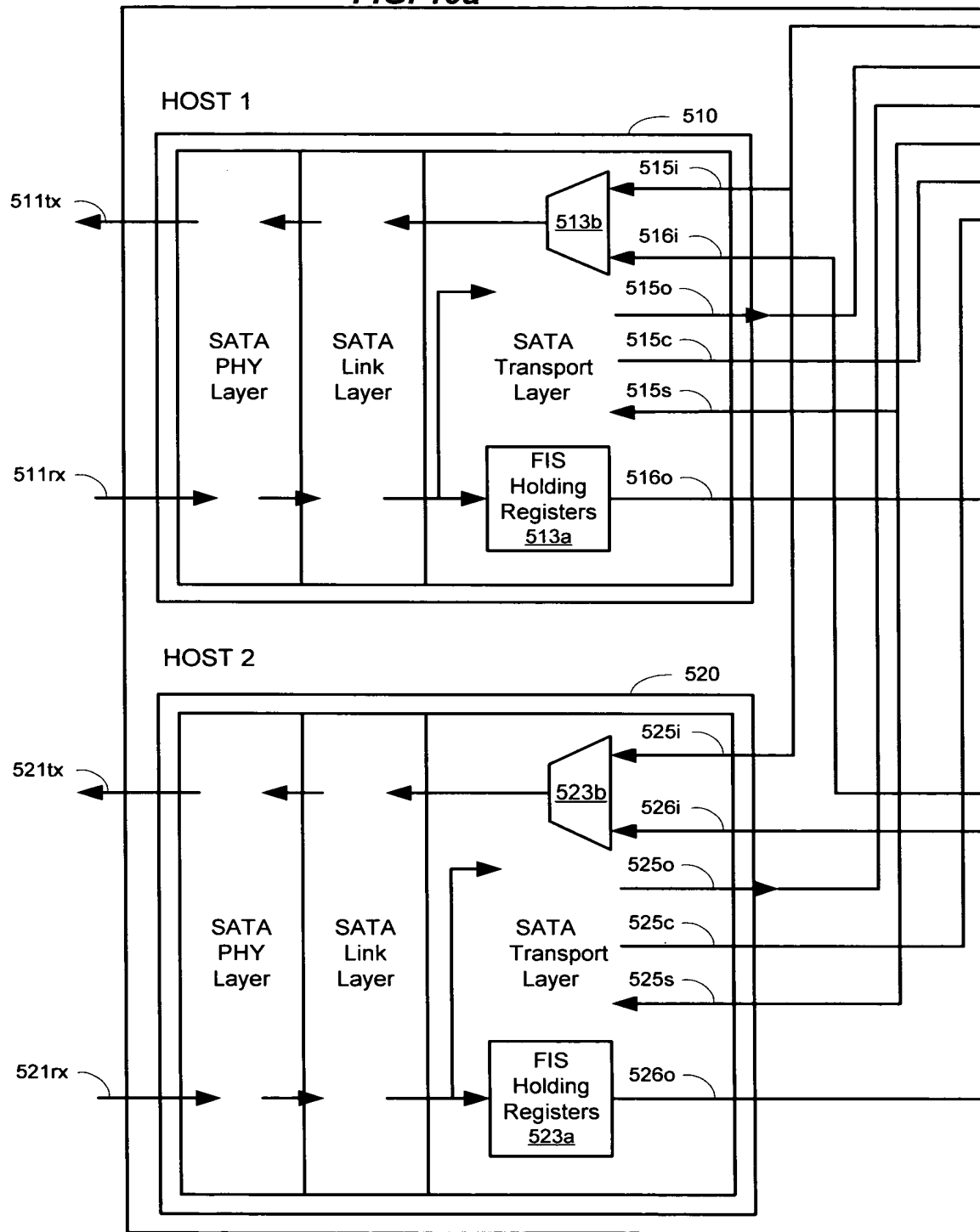


FIG. 10a(i)

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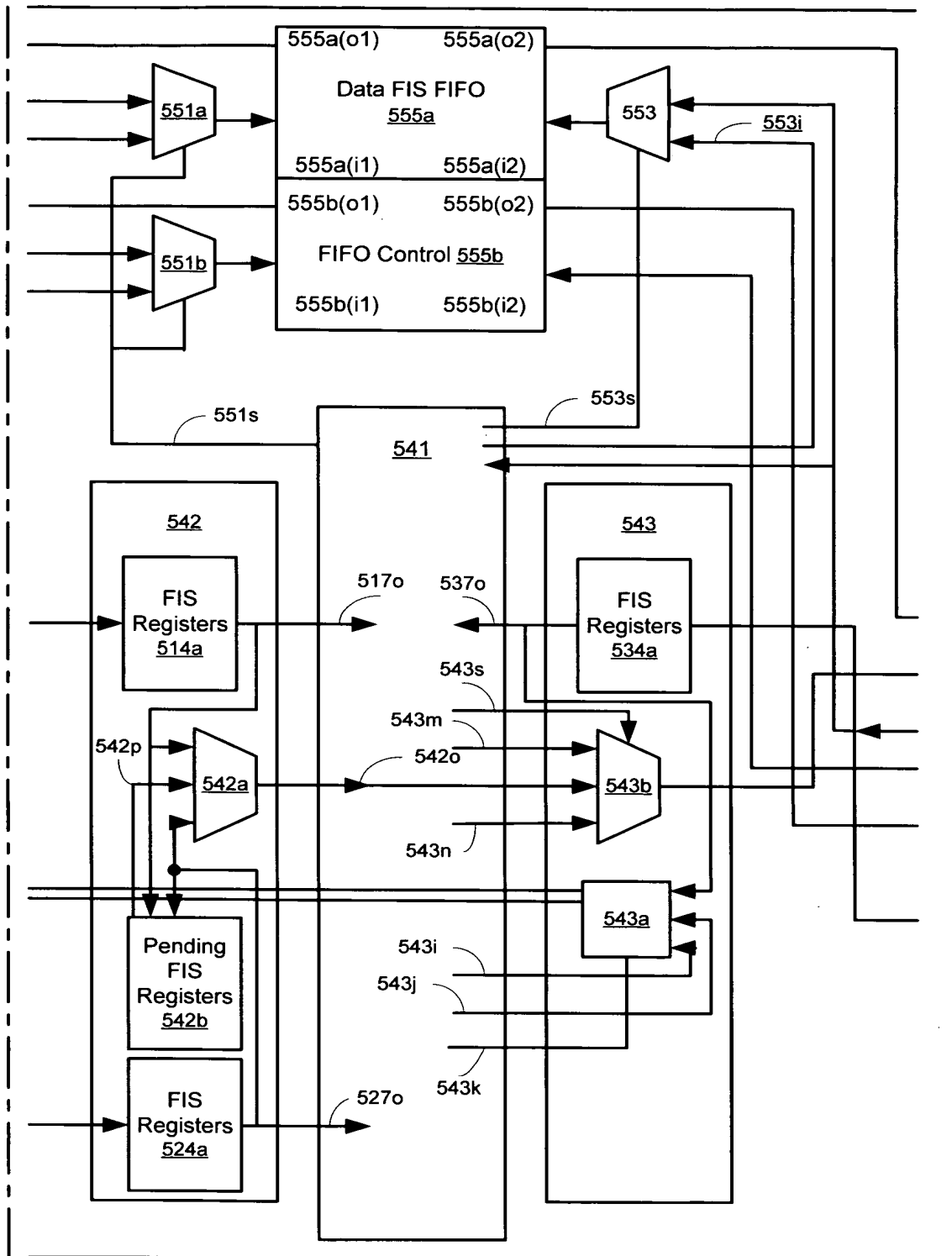


FIG. 10a(ii)

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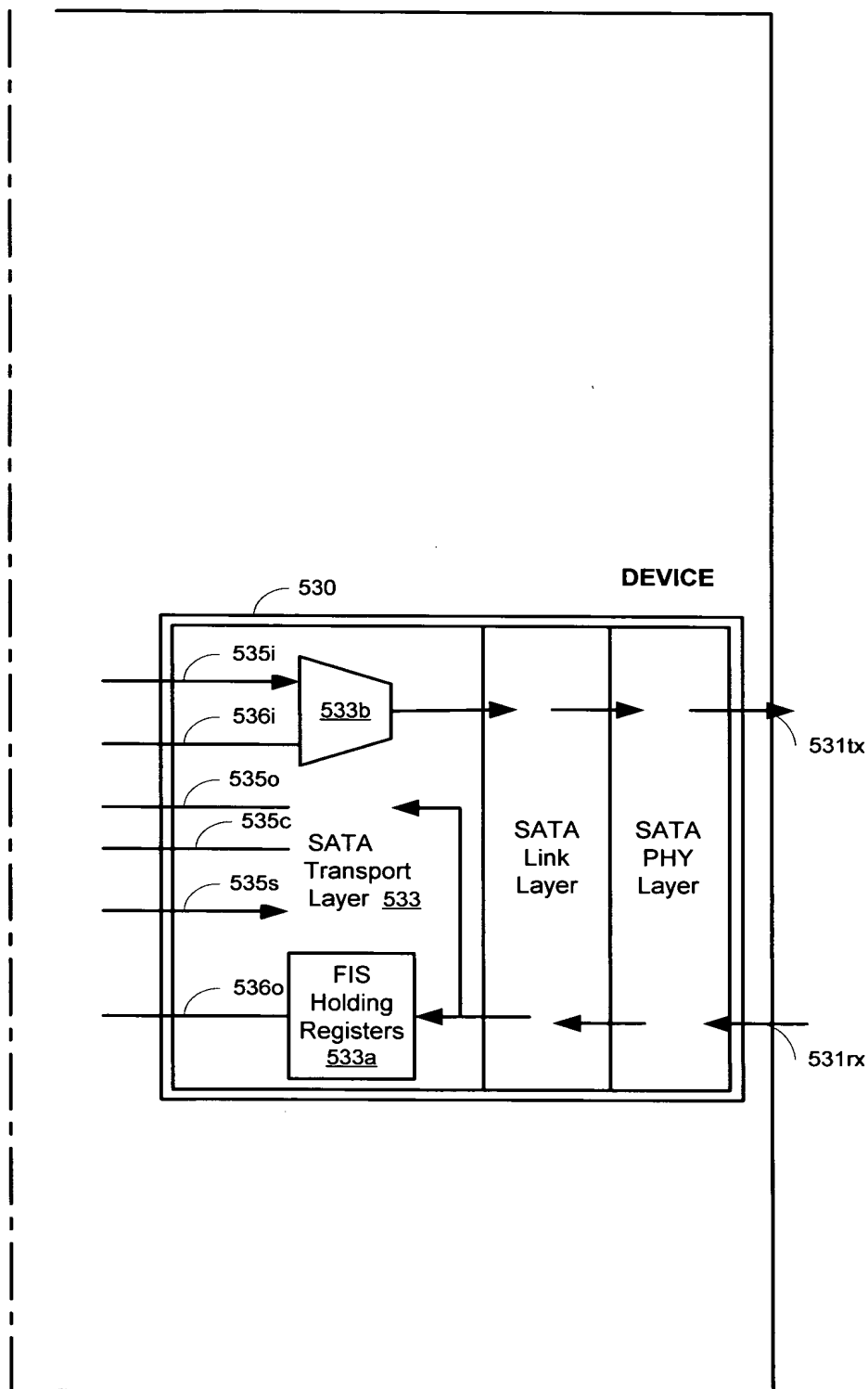


FIG. 10a(iii)

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FIG. 10b(i)

FIG. 10b(ii)

FIG. 10b(iii)

Key to

FIG. 10b

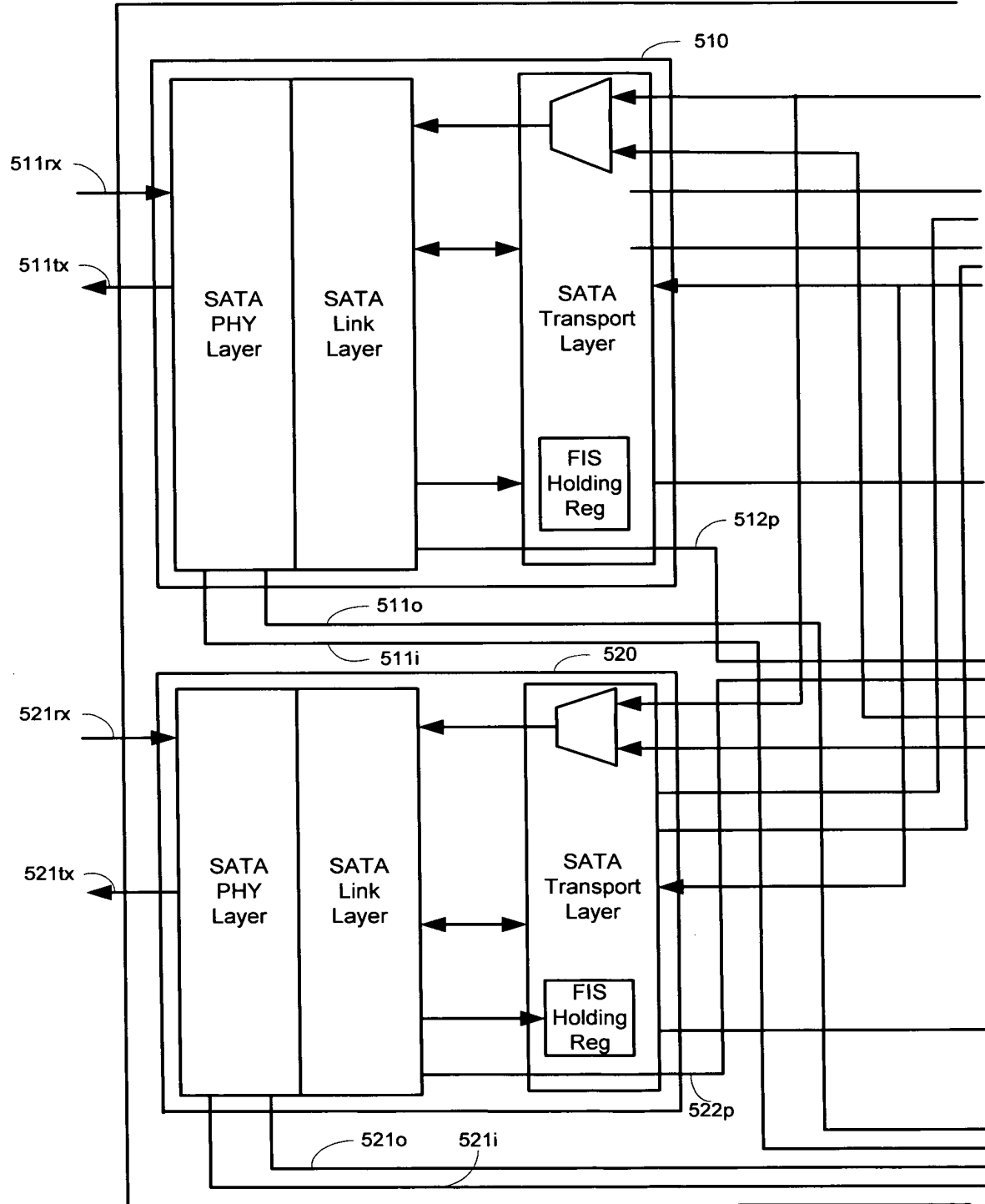


FIG. 10b(i)

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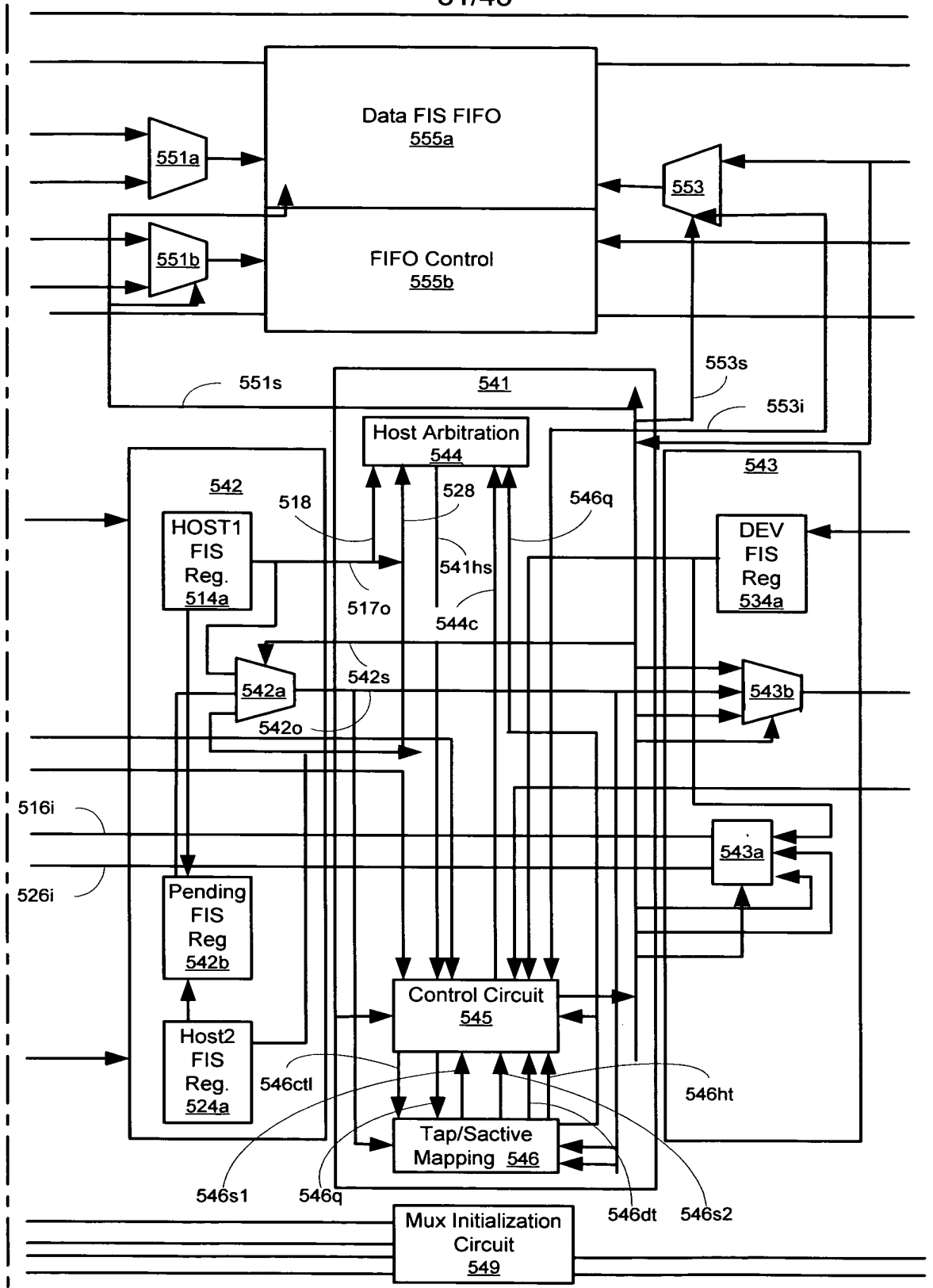


FIG. 10b(ii)

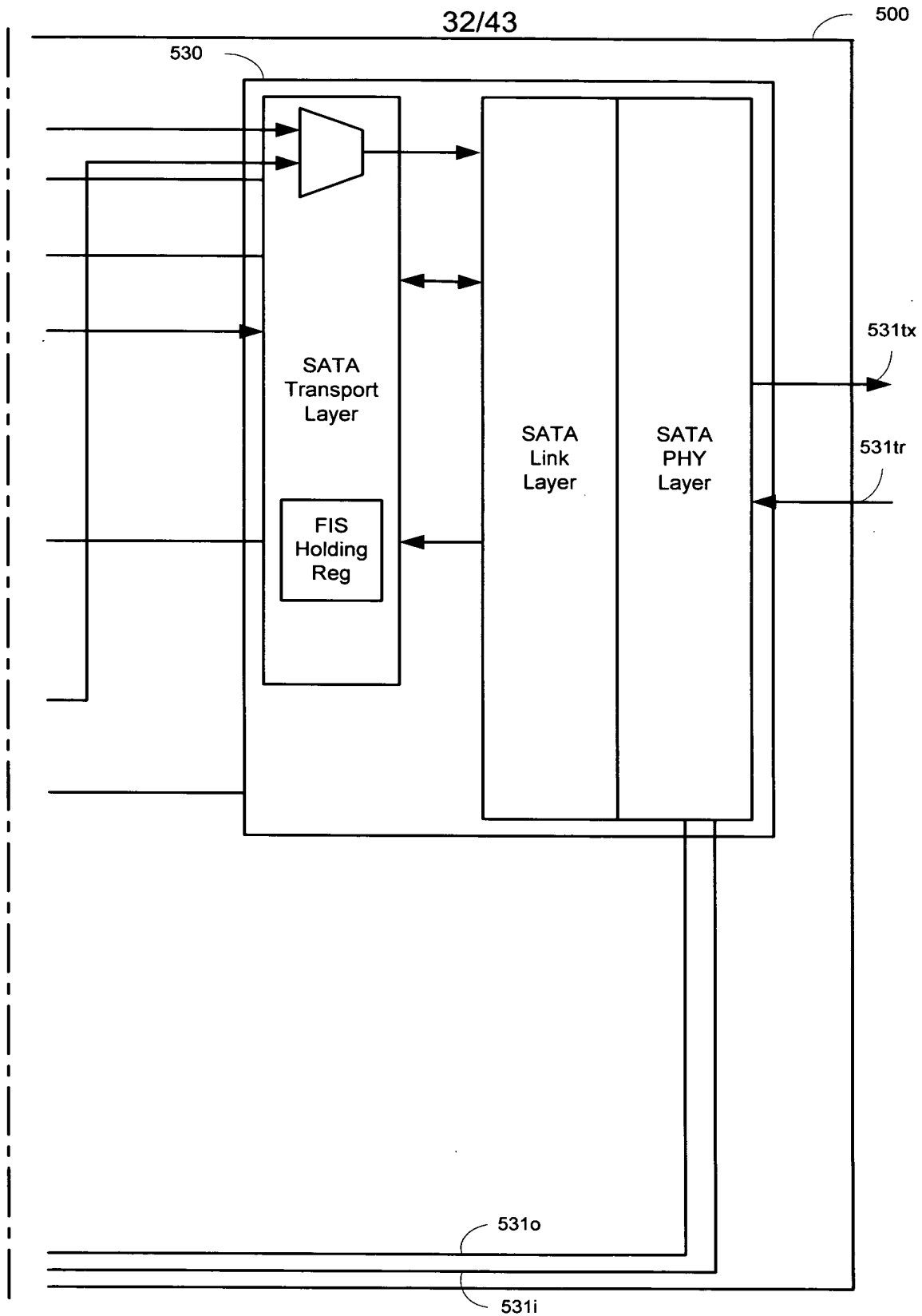


FIG. 10b(iii)



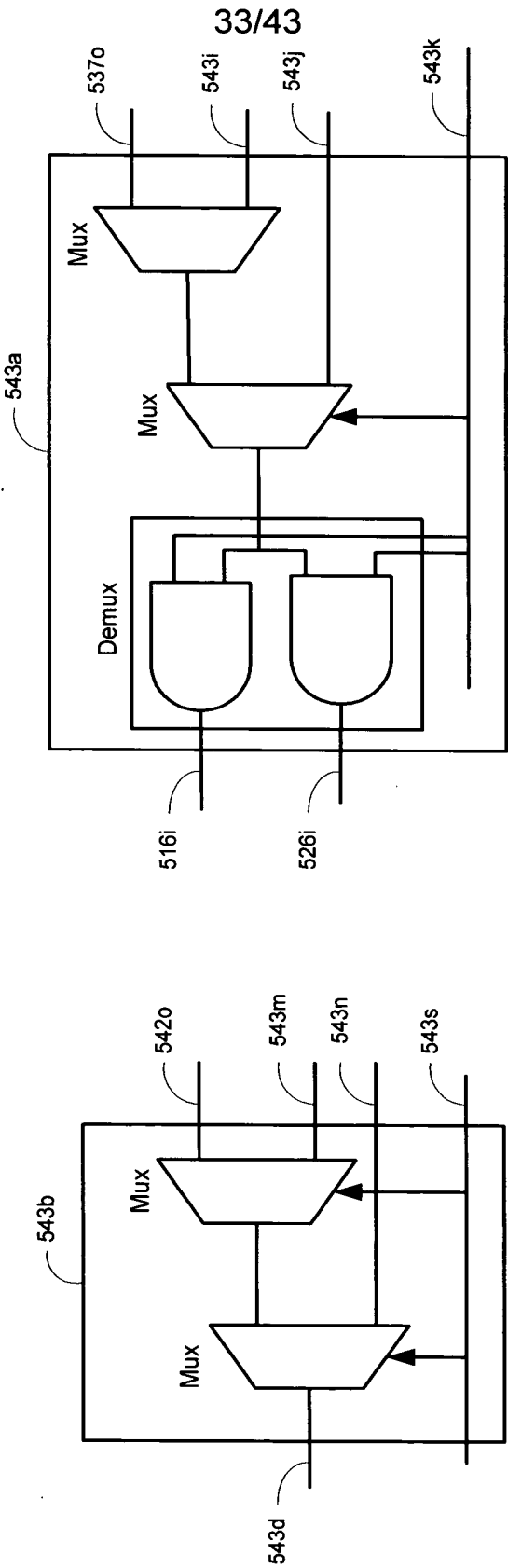
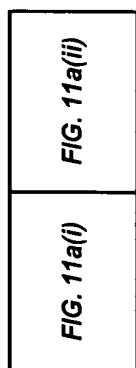


FIG. 10c



Key To

FIG. 11a

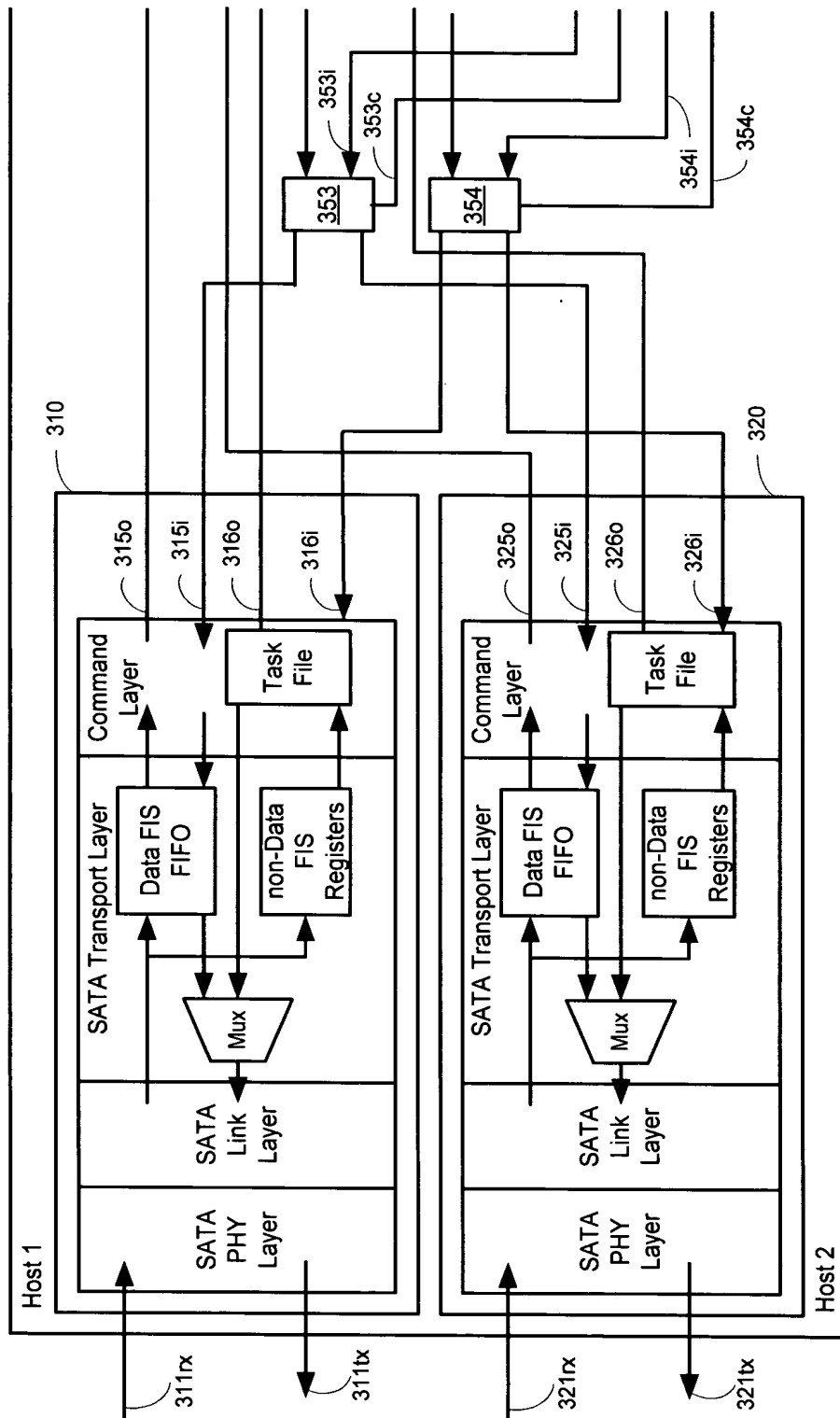


FIG. 11a(i)

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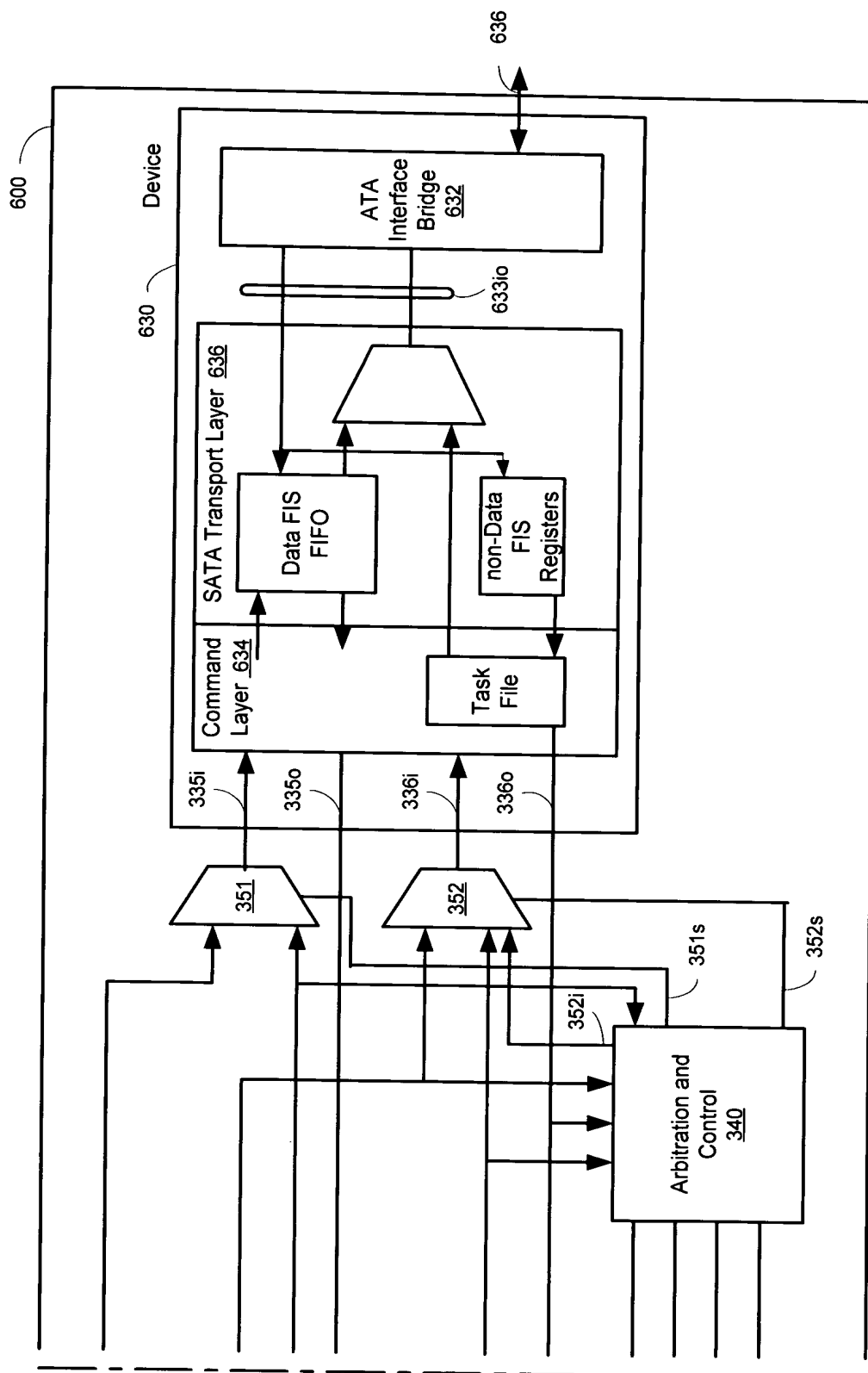


FIG. 11a(ii)

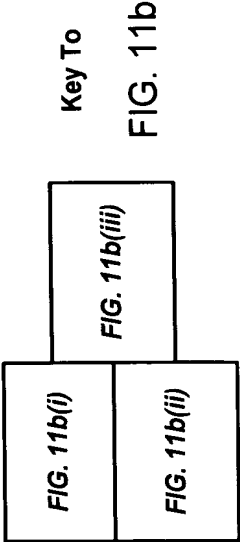


FIG. 11b

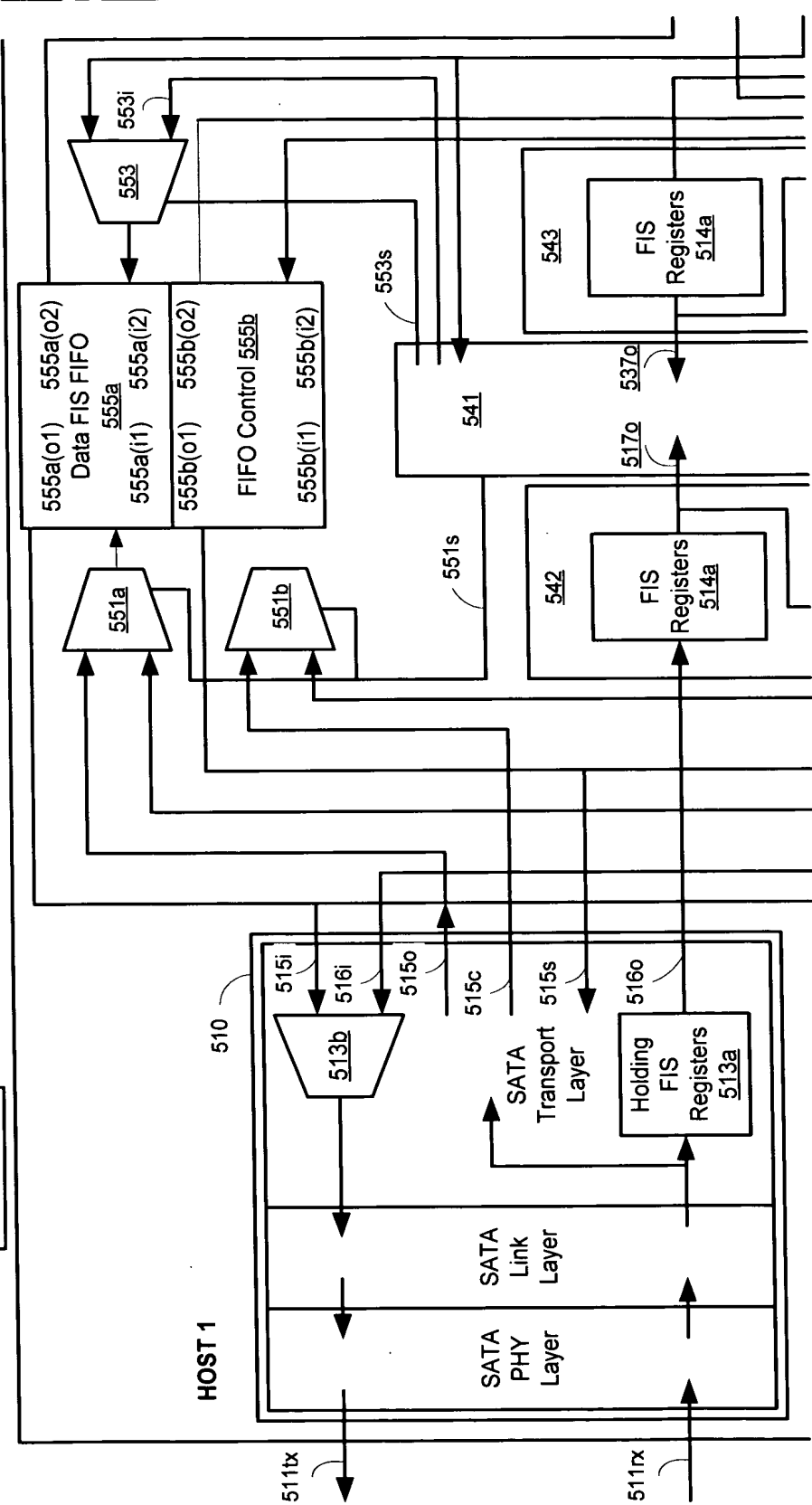
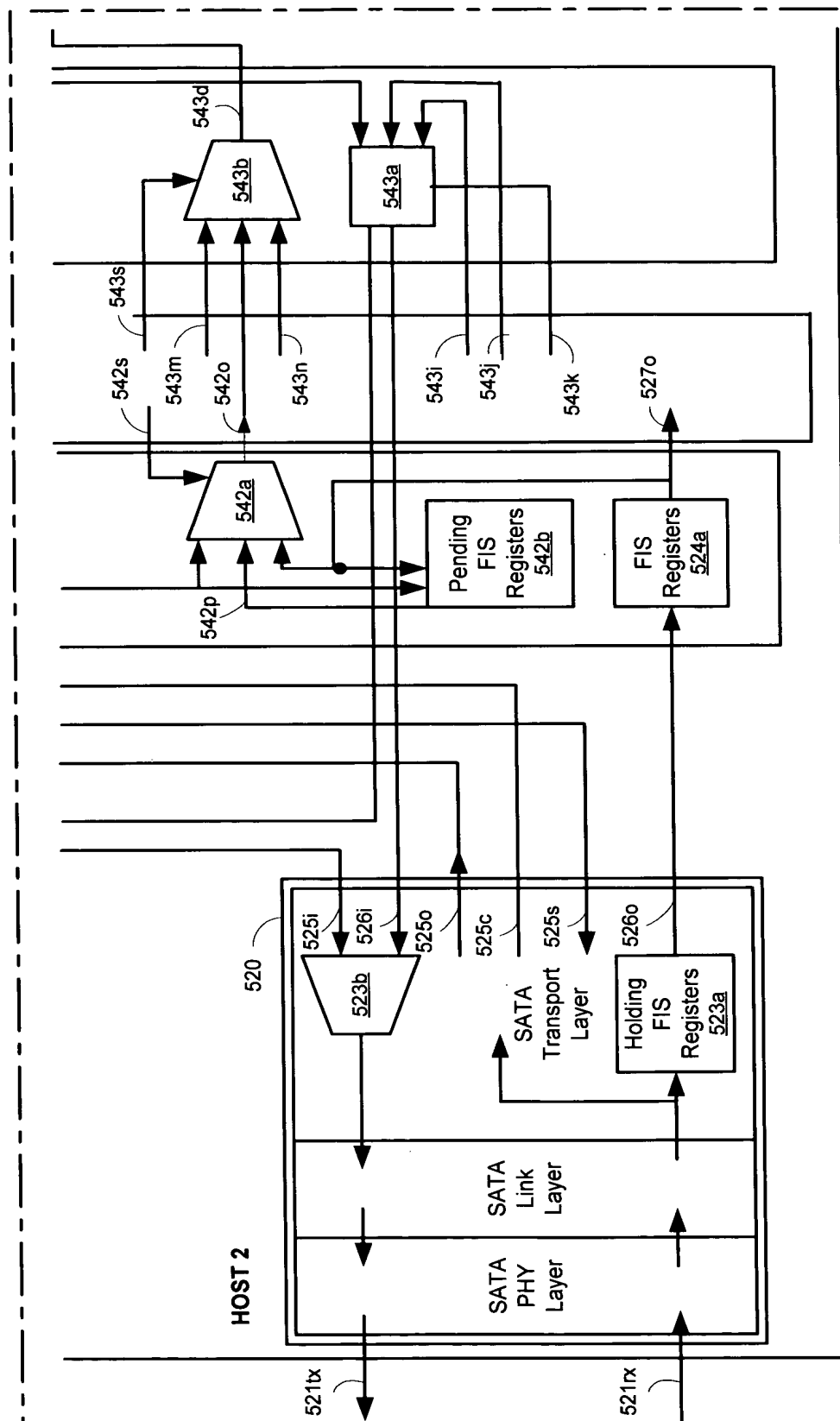


FIG. 11b(i)

**FIG. 11b(ii)**



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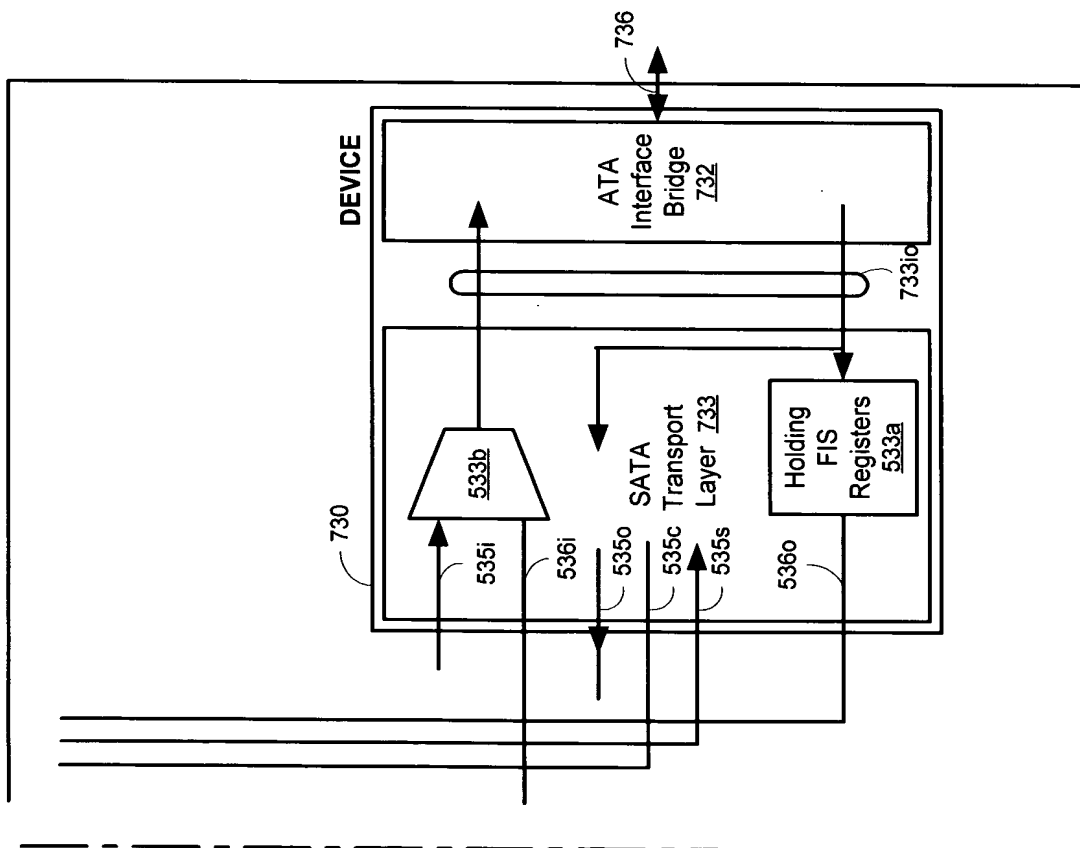


FIG. 11b(iii)

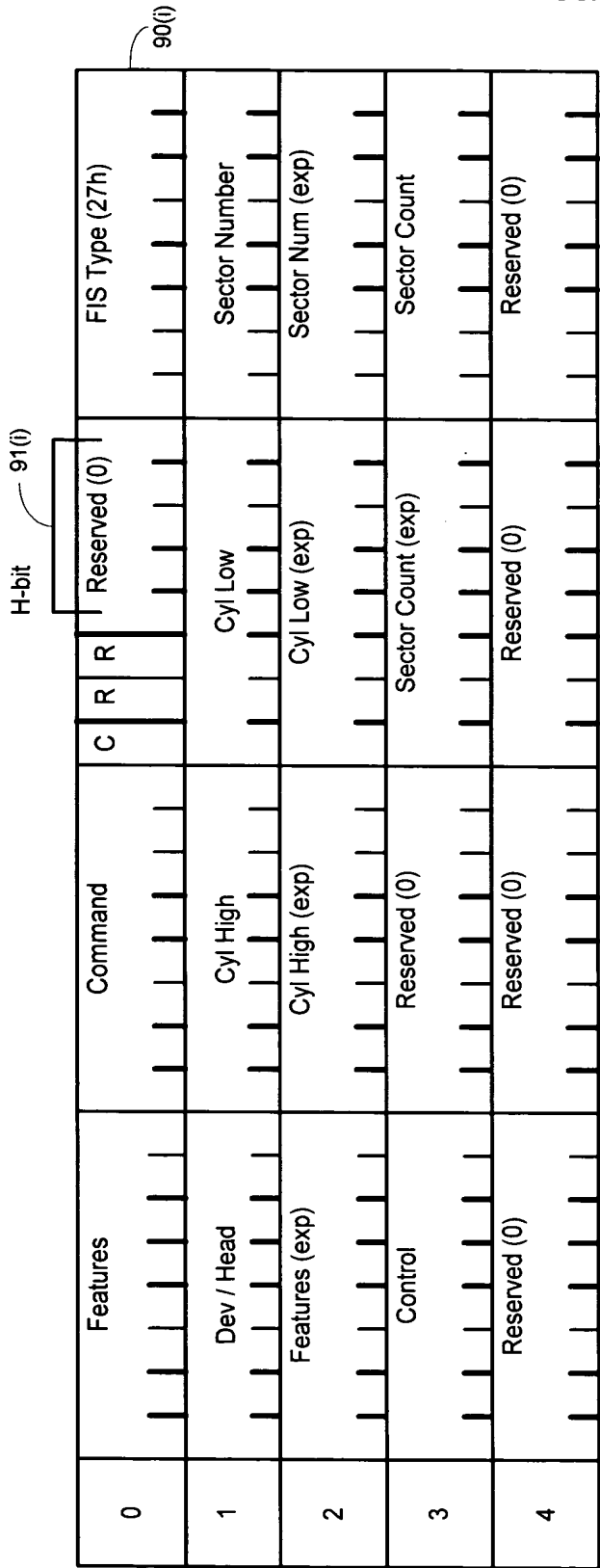


FIG. 12(i) Register FIS Host to Device

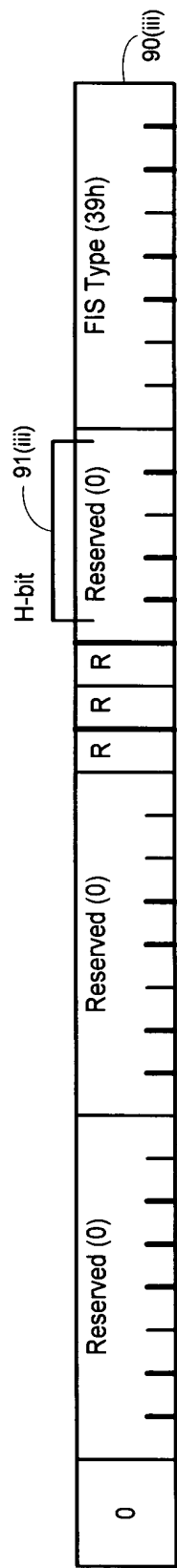


FIG. 12(iii) DMA Activate FIS, Device to Host

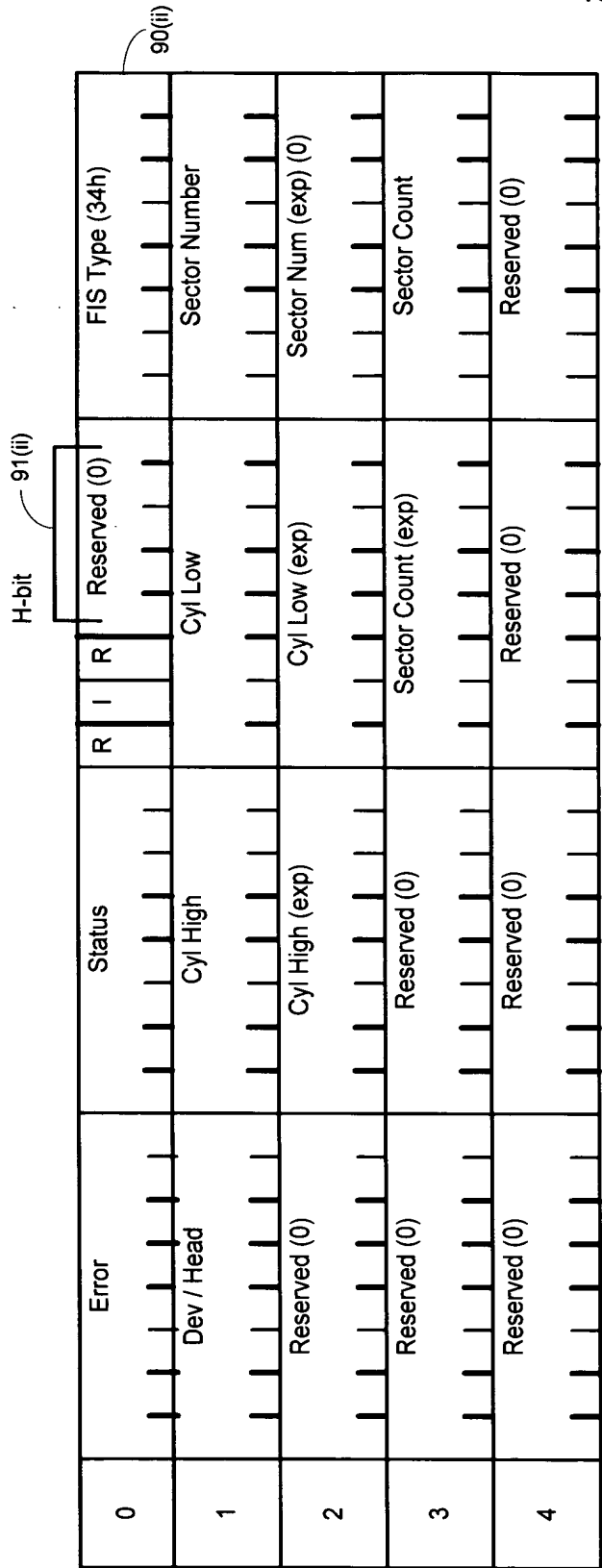


FIG. 12(ii) Register FIS Device to Host

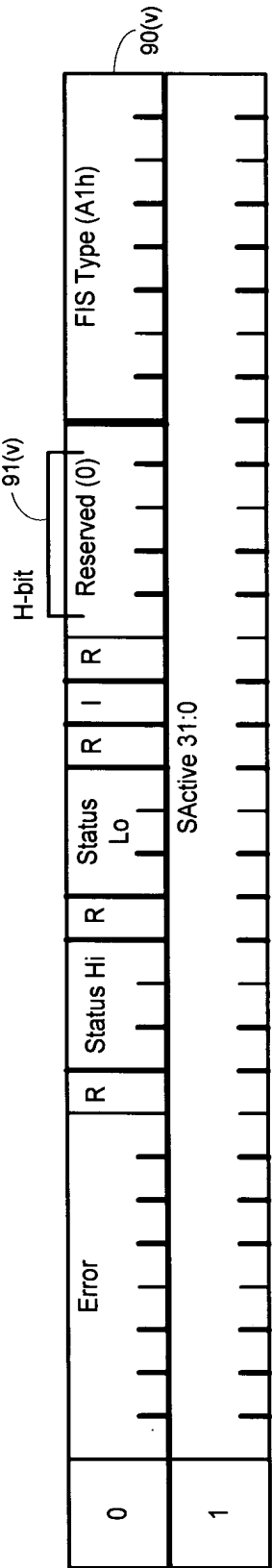


FIG. 12(v) Set Device Bits FIS



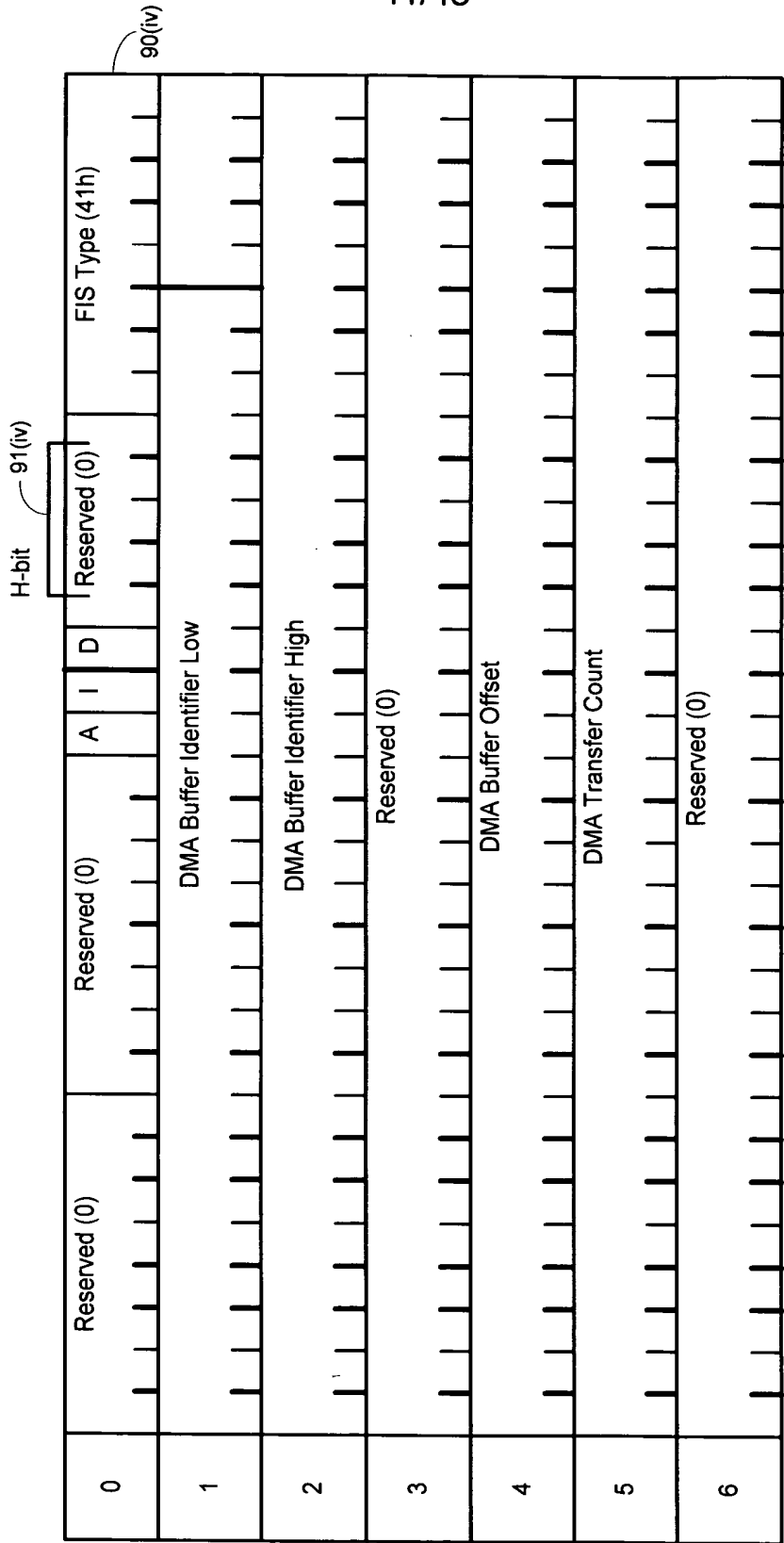


FIG. 12(iv) DMA Setup FIS

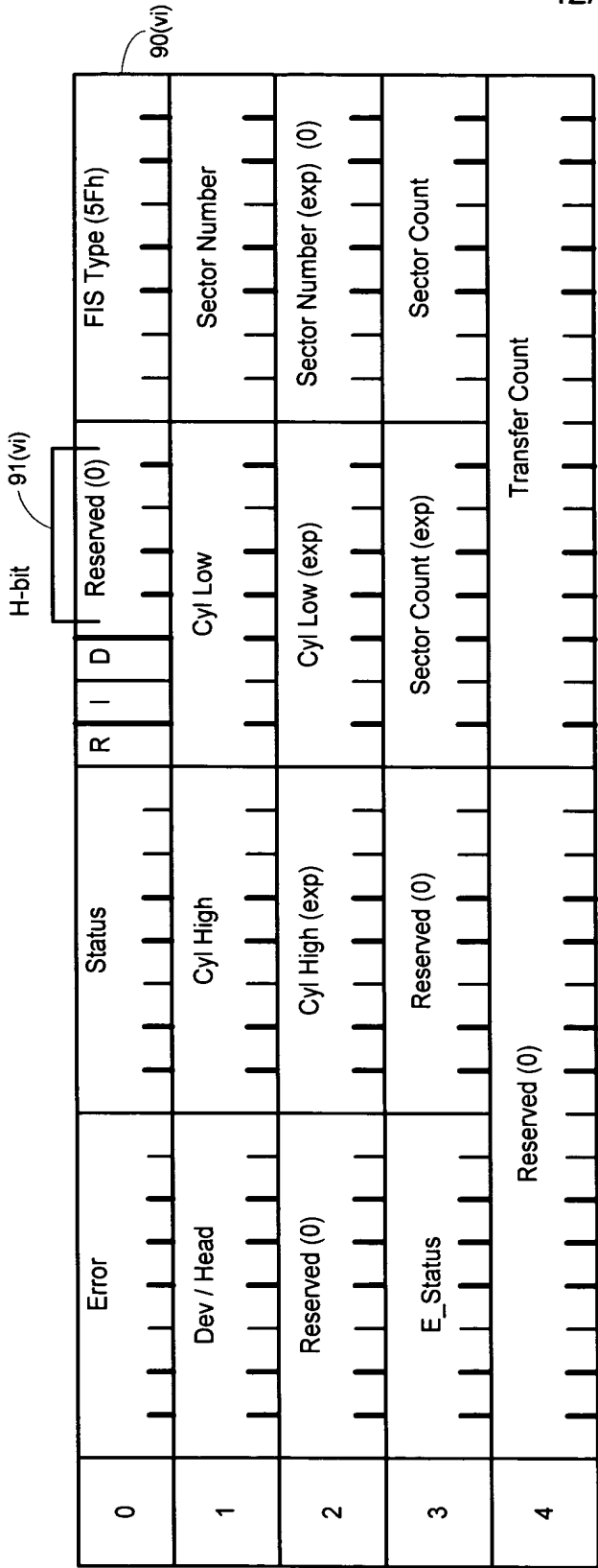


FIG. 12(vi) PIO Setup FIS

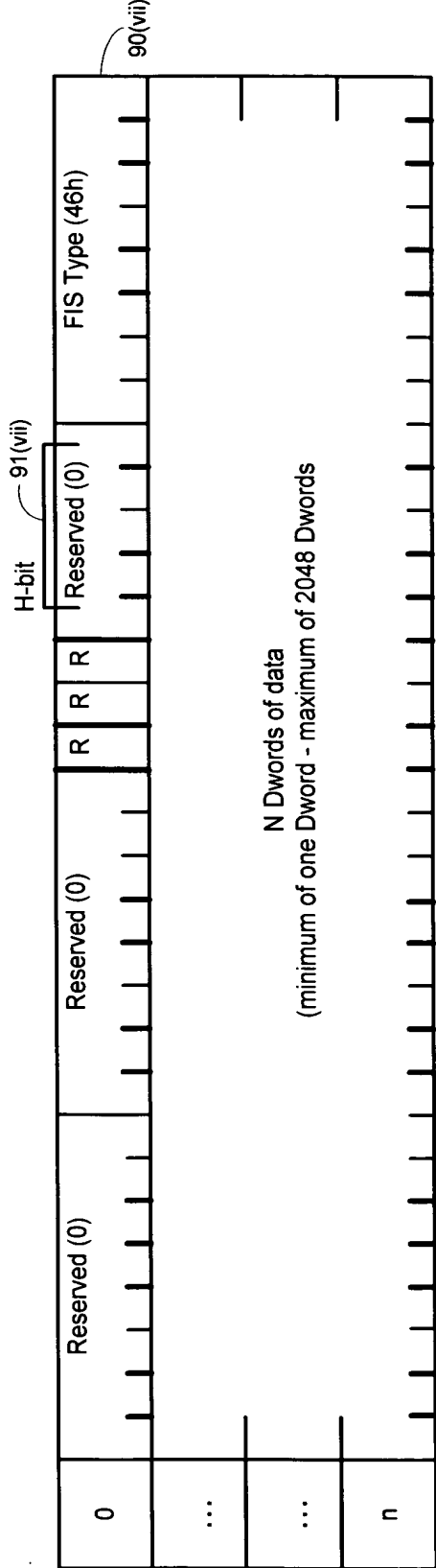


FIG. 12(vii) Data FIS

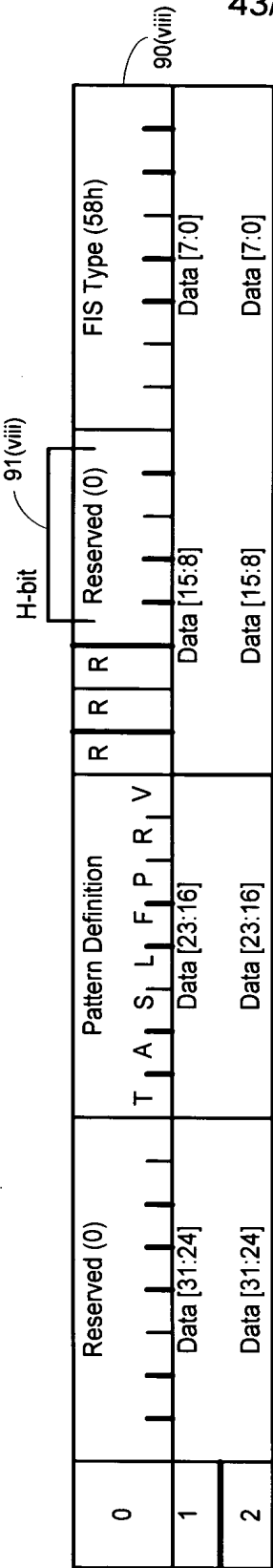


FIG. 12(viii) BIST Activate FIS